

A TWO DAY WORKSHOP  
ON  
**ANALOG VLSI DESIGN**  
BRIDGING GAP BETWEEN CLASSROOM AND  
INDUSTRY

**Registration Form**

Name: \_\_\_\_\_

Designation: \_\_\_\_\_

Gender: \_\_\_\_\_

Organization: \_\_\_\_\_

Address for Correspondence: \_\_\_\_\_

\_\_\_\_\_

\_\_\_\_\_

Phone/Mobile: \_\_\_\_\_

Email: \_\_\_\_\_

Education Qualification: \_\_\_\_\_

Experience: \_\_\_\_\_

Category: Academic / Industry / R&D: \_\_\_\_\_

**Payment Details:**

Draft No: \_\_\_\_\_ Date: \_\_\_\_\_

Drawn on: \_\_\_\_\_

Amount Rs. \_\_\_\_\_

Place: **Applicant's Signature**

Date:

**Signature of Head of the Institute / Organization with Seal**

For online registrations visit :

<https://sites.google.com/view/cbit-analog-vlsi-workshop-2017/home>

**Patron:**

**Dr. V. Malakonda Reddy**  
President,  
CBIT Society

**Advisors:**

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Principal CBIT

**Dr. Kaleem Fatima**  
Chapter Chair, IEEE CAS/EDS, Hyderabad Section.

**Workshop Chairman:**

**Dr.N.V. Koteswara Rao**  
HEAD - Dept. of ECE, Dean CDAAC

**Coordinator:**

**Mohd Ziauddin Jahangir,**  
Asst. Prof., Dept. of ECE, CBIT

**Co-Coordinator:**

**P. Chandrasekar,**  
Asst. Prof., Dept. of ECE, CBIT

**Course Fee:**

	IEEE members	Others
BE / ME Students	Rs. 200 /-	Rs. 250/-
PhD Scholars	Rs. 300/-	Rs. 350/-
Faculty	Rs. 400 /-	Rs. 500/-
Industry	Rs. 600/-	Rs. 800/-

**Payment Mode:**

Demand draft in favor of 'Head, Department of ECE'  
payable at Andhra Bank, Kokapet Branch, Hyderabad.

**Important Dates:**

Last date for receipt of application: **11<sup>th</sup> Mar, 2017**

Intimation to selected candidates: **13<sup>th</sup> Mar, 2017**

**For further details please contact:**

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A Two Day Workshop  
on

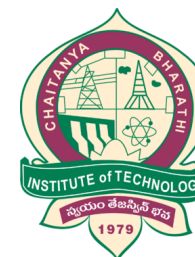
**Analog VLSI Design**

**Bridging Gap between  
Classroom and Industry**

*Jointly Organized by*

**CBIT &**

**Joint Chapter of CAS/EDS societies,  
IEEE Hyderabad**



*Supported by*

**TEQIP II**

**17<sup>th</sup> - 18<sup>th</sup> March, 2017**

*Venue: E-ClassRoom, CBIT*

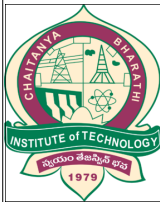
*Dept. of Electronics & Communication Engg  
Chaitanya Bharathi Inst. of Technology (A)*

*Accredited by NBA-AICTE, Accredited by NAAC-*

*UGCSO 9001:2008 Certified Institution,*

*Gandipet, Hyderabad – 500 0075*

# CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY (CBIT)



CBIT is one of the premier engineering colleges for imparting engineering education in the state. This is a first self-financed engineering college, established in 1979 in Hyderabad with a prime motto to shape young, innovative and creative engineers in building the Nation's Human

Resource Capital. The college offers Nine UG and Eleven PG courses. It has been accredited by NBA (AICTE) and NAAC (UGC). This institute is also certified by ISO 9001:2008. Autonomous status was granted by UGC from the academic year 2013-14. The grants received from AICTE/UGC are worth about Rs.2.0 crores. The Institute has signed MOU with State Project Facilitation Unit (SPFU), Technical Education Quality Improvement Program (TEQIP-II) Hyderabad. The objectives of the TEQIP project are strengthening institutions to produce high quality engineers for better employability, Scaling-up PG education, Demand-Driven Research and development and innovation, Establishing centers of excellence for focused applicable research, training of faculty for effective teaching and enhancing institutional and system management effectiveness.

## DEPT. OF ECE

The department of ECE was established in 1979. The department offers Bachelor of Engineering (BE) in ECE. This is accredited by NBA (AICTE). Also offers two Master of Engineering (ME) programs with Communication Engineering and Embedded Systems & VLSI Design as specializations. The department has highly qualified and experienced faculty. The department has good infrastructural facilities and eleven full-fledged laboratories equipped with adequate hardware and software.

The faculty is active in R&D and publishing papers in International / National Journals and Conferences. The department has successfully completed projects from AICTE and GE.

Presently the department is executing projects that are sponsored by AICTE (New Delhi), DST (New Delhi), and RCI (DRDO). So far this department organized 32 technical programs including Faculty development program (FDP) and National Seminar (NS) sponsored by AICTE. The Dept. is recognized as a Research Center by Osmania University, Hyderabad.

## JOINT CHAPTER OF CAS/ EDS SOCIETIES, IEEE HYDERABAD SECTION



IEEE Hyderabad Section was established in 1980 and has been a very active section in Asia Pacific region. It was awarded the large section award in year 2015. There are 10 Technical Societies, 2 affinity groups and one Technology management council in the Hyderabad section.

The Joint Chapter of IEEE Circuits and Systems/ Electron Device Societies was established in 2011 by a team of dedicated volunteers from Industry and Academia. IEEE CAS/EDS Hyderabad has successfully hosted PrimeAsia 2012, PrimeAsia 2013 and PrimeAsia 2015. The chapter has established good rapport with IEEE CAS Japan, Singapore, Malaysia and Indonesia over the last three years utilizing the CASS Networking initiative and has conducted workshops and conferences in collaboration with these countries. The CAS chapter is motivated to place Hyderabad section on the map of circuits world by organizing distinguished conferences like APCCAS, ISCAS and others.

## ABOUT THE WORKSHOP

This Workshop Aims at bridging gap between the classroom design procedures and the desired specifications and limitation of the fabrication industry. Economics governing the design of ICs needs to be known to the designer so that the specifications framed are realizable and circuit performance is reasonable after fabrication. How the Layout and Pin placement has to planned and their impact on design will be discussed.

What are ESD/ EMC issues and their impact on the design. What is the validation process used to verify the design. These are called as Environment variables of an Analog IC Design. This workshop aims at making the students aware of the initial environment variables that govern the domain of Analog Design.

Suppose a student is asked to solve a design problem from a text book. A lot of inputs will be readily available in the question itself, For an example, it is asked to design an Amplifier, then the type of amplifier, required gain, etc will be given so that a student readily uses the design equation and designs them. What he misses to know is, How are these specifications derived? Why to use that particular Amplifier topology? Will the final designed circuit Work? Will it be economical to fabricate? Will it work even in worst cases?

The Answers to above questions, is the expected take-away from this workshop.

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### RESOURCE PERSONS

#### **Dr. P. Chandra Sekar**

Assoc. Prof., Dept. of ECE,  
OUCE

#### **Sri. A.G. Krishnakanth,**

Senior Manager – (BL AOS Engg ),  
AMS Semiconductors India Pvt Ltd

#### **Sri. Rohit Ranganathn ,**

Team Leader (Analog),  
AMS Semiconductors India Pvt Ltd

#### **Sri. Ravi Kumar ,**

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AMS Semiconductors India Pvt Ltd

#### **Sri. Sridhar Setty ,**

Senior Engineer (Analog),  
AMS Semiconductors India Pvt Ltd