CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY
Autonomous Institution under UGC
Hyderabad-500 075 -T.S.

DEPARTMENT OF
ELECTRONICS & COMMUNICATION ENGINEERING

Scheme of Instruction
And
Syllabi of

M.E. (ECE)

Embedded Systems & VLSI Design

(With effect from 2016-2017)

CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
(Autonomous)

VISION AND MISSION OF THE INSTITUTE

Vision

To be a centre of excellence in technical education and research.

Mission

To address the emerging needs through quality technical education and advanced research.

VISION AND MISSION OF THE DEPARTMENT

Vision

To develop the department into a full-fledged centre of learning in various fields of Electronics & Communication Engineering, keeping in view the latest developments.

Mission

To impart value based technical education and train students and to turn out full fledged engineers in the field of Electronics & Communication Engineering with an overall background suitable for making a successful career either in industry/research or higher education in India/Abroad.

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Scheme of Instruction & Examination
M.E Four Semester Course (Regular) 2016-2017

I- SEMESTER

Course Code	Subject	No. of Hrs./Week		Marks for		Total Marks	Credits
		Lecture	T/P/S	Internal Assessment	End Exam		
	Core 1	3	1	30	70	100	4
	Core 2	3	1	30	70	100	4
	Core 3	3	1	30	70	100	4
	Elective 1	3	--	30	70	100	3
	Elective 2	3	--	30	70	100	3
	Elective 3	3	--	30	70	100	3
16EC C207	Lab 1	---	3	50	-	50	2
16EC C209	Seminar 1	---	3	50	-	50	2
16EC C211	Soft Skills	---	2	--	-	-	-
Total		18	11	280	420	700	25

Soft Skills is included as a non-credit course in the I-semester

II-SEMESTER

Course Code	Subject	No. of Hrs./Week		Marks for		Total Marks	Credits
		Lecture	T/P/S	Internal Assessment	End Exam		
	Core 4	3	1	30	70	100	4
	Core 5	3	1	30	70	100	4
	Core 6	3	1	30	70	100	4
	Elective 4	3	---	30	70	100	3
	Elective 5	3	---	30	70	100	3
	Elective 6	3	---	30	70	100	3
16EC C208	Lab 2	---	3	50	-	50	2
16EC C210	Seminar 2	---	3	50	-	50	2
16EC C212	Mini Project	---	2	50	-	50	1
Total		18	11	330	420	750	26

III-SEMESTER

Course Code	Subject	Marks for		Total Marks	Credits
		Internal Assessment	End Exam		
16EC C213	Project work-Project Seminar (i) Problem formulation and submission of synopsis within 8 weeks from the commencement of 3rd semester. (50 Marks) (ii)Preliminary work on Project Implementation. (50 Marks)	100	----	100	6
Total		100		100	6

IV-SEMESTER

Course Code	Subject	Marks for		Total Marks	Credits
		Internal Assessment	End Exam		
16EC C214	Project work and Dissertation	100	100	200	12
Total		100	100	200	12

Industrial Training / Internship

The students may undergo Industrial training/Internship during summer / winter vacation. In this case the training has to be undergone continuously for the entire period.

The students may undergo Internship at Research organization / University (after due approval from the Head of the Department) during summer / winter vacation or during semester break.

Duration of Training/ Internship	Credits
2 Weeks	1
4 Weeks	2

If Industrial Training / Internship are not prescribed in the curriculum, the student may undergo Industrial Training / Internship optionally and the credits earned will be indicated in the Mark Sheet.

However, credits earned due to internships **shall not be considered** for dropping any course or in process of award of degree. The student is allowed to undergo a maximum of 6 weeks Industrial Training / Internship during the entire duration of study, no credits will be allotted for the internship beyond six(6) weeks.

The detailed procedures are furnished in the **ANNEXURE** regarding the earning of credits by the student for **Industrial Training / Internship**

Industrial Visit

Every student is required to go for at least one industrial visits during the I-semester /II--semester of the Programme. The Heads of Departments shall ensure that necessary arrangements are made in this regard. **It is non-credit course and is awarded with 'Satisfactory/Un-satisfactory' and will be reflected in grade sheet.**

List of Subjects for ME (ECE) Course with specialization in EMBEDDED SYSTEMS & VLSI DESIGN W.E.F. 2016-2017

S.No	Syllabus Ref. No	Subject	Hours per week
Core Subjects			
1	16EC C201	Microcontrollers for Embedded System Design	4
2	16EC C202	CMOS VLSI Design	4
3	16EC C203	RF IC Design	4
4	16EC C204	Embedded Processors and Architecture	4
5	16EC C205	Analog and Mixed Signal IC Design	4
6	16EC C206	Real Time Operating Systems	4
7	16EC C207	Lab-1-Design and Simulation Laboratory-I	3
8	16EC C208	Lab-2-Design and Simulation Laboratory-II	3
9	16EC C209	Seminar - 1	3
10	16EC C210	Seminar - 2	3
11	16EC C211	Soft Skills	2
12	16EC C212	Mini Project	2
13	16EC C213	Project work -Project Seminar	--
14	16EC C214	Project work and Dissertation	--
Elective Subjects			
15	16EC E215	Computer Communication Networks	3
16	16EC E216	Embedded System Design	3
17	16EC E217	Advanced Computer Organization	3
18	16EC E218	CPLD & FPGA Architectures and Applications	3
19	16EC E219	Design For Testability	3
20	16EC E220	VLSI Technology	3
21	16EC E221	Low Power VLSI Design	3
22	16EC E222	VLSI Signal Processing	3
23	16EC E223	Advanced Digital Design with Verilog HDL	3
24	16EC E224	VLSI Physical Design Automation	3
25	16EC E225	System on Chip Architecture	3
26	16EC E226	Physics of Semiconductor Devices	3
27	16EC E227	Optimization Techniques	3

16EC C201

MICROCONTROLLERS FOR EMBEDDED SYSTEMS DESIGN

Instruction	4 Hours per week	End Exam- Duration	3 Hours
Sessionals	30 Marks	End Exam- Marks	70 Marks

UNIT-I

Introduction to Embedded Systems: Review of Microprocessors and their features. Differences between Microprocessors and Microcontrollers, Application areas of Embedded Systems, Categories of Embedded Systems.Overview of Embedded System Architecture, Challenges & Trends of Embedded Systems, Hardware Architecture, Software Architecture.

UNIT-II

Architecture, Instruction Set, Addressing Modes, ALP, Timers and Counters, Serial Communication, Interrupt Programming of 8051. Interfacing with External Memory, Expansion of IO Ports.Introduction to embedded cross compilers.

UNIT-III

Interfacing 8051 with ADC, DAC, LCD and Stepper Motor.PIC 18 Family Overview, Architecture, Instruction Set, Addressing modes, Timers and Interrupts of PIC 18.

UNIT-IV

Capture/Compare and PWM modules of PIC 18.Introduction to RISC Concepts with ARM Processor.Embedded Software Development Tools, Host and Target Machines, Linkers/Locators for Embedded Software, Getting Embedded Software into the Target System.

UNIT-V

Debugging Techniques- Testing on your Host Machine, Instruction Set Simulators, Using Laboratory Tools.

Case Studies: Design of Embedded Systems using Microcontrollers – for applications in the area of communications and automotives. (GSM/GPRS, CAN ,Zigbee)

Suggested Readings:

1. David.E.Simon , "An Embedded Software Primer" Pearson Education.
2. Mazidi M.A and Mazidi J.G, "The 8051 Microcontroller and Embedded Systems" , Pearson 2007.
3. Mazidi, MCKinlay and Danny Causey, "PIC Microcontrollers and Embedded Systems", Pearson Education.
4. Raj Kamal,Embedded Systems – Architecture, Programming and Design ,2nd Edition, TMH, 2008.

16EC C202

CMOS VLSI Design

Instruction	4 Hours per week	End Exam- Duration	3 Hours
Sessionals	30 Marks	End Exam- Marks	70 Marks

UNIT I: Introduction

Introduction to VLSI System design hierarchical design – design abstraction – different levels of abstraction and domains. MOS Transistor theory- NMOS inverter and logic gates-CMOS inverter and logic –Transmission gate logic design-Differential CMOS logic circuits.

UNIT II: Advanced CMOS Logic Design

Static CMOS Digital Latches- dynamic CMOS latches-CMOS Flip-flops- pseudo NMOS and dynamic pre-charging, domino- CMOS logic, no race logic, single-phase dynamic logic, dynamic differential logic.

UNIT III: Logic Families and Building Blocks for Digital Design

Emitter coupled logic gates - current mode logic gates - BiCMOS Logic gates, Building blocks for digital design: multiplexer, demultiplexer, decoder, encoder -Barrel Shifter-Counters-Digital Adders-Multipliers-Parity generators-Detectors-Comparators.

UNIT IV: Memory and Programmable Logic

CMOS design methods: Structured design strategies – Hierarchy, regularity modularity, SRAM-Sense amplifier-address buffer and decoder, DRAM, ROM, Logic Arrays- PLA, PAL, Gate Arrays-FPGA, Design for testability

UNIT V: System Case Studies

Finite State Machine (FSM), Algorithmic State Machines (ASMS), synchronization failure and meta stability, CMOS System case study: Core of RISC Micro Controller ALU address architectures.

Suggesting Readings:

1. Ken Martin, “Digital Integrated Circuit Design”, Oxford University Press 2000.

2. Weste Kamran Eshraghian, Principles of CMOS VLSI design – a Systems Perspective by

NEILHE, Pearson Education Series, Asia 2002.

3. John P. Uyemura, “Introduction to VLSI Circuits and systems”, John Wiley & Sons, 2011.
4. Sung-Mo Ang& Yusuf Leblebigi , “CMOS Digital Integrated Circuits Analysis and Design”- Mc-Gra-Hill Higher Education, 2nd Edition2003.

16EC C203

RF IC Design

Instruction	4 Hours per week	End Exam- Duration	3 Hours
Sessionals	30 Marks	End Exam- Marks	70 Marks

Unit I:

RF systems – basic architectures, Transmission media and reflections, Maximum power transfer, Passive RLC Networks, Parallel RLC tank, Q ,Series RLC networks, matching, Pi match, T match , Passive IC, Interconnects and skin effect, Resistors, capacitors, Inductors.

Unit II:

Review of MOS Device Physics, MOS device review , Distributed Systems ,Transmission lines, reflection coefficient, The wave equation, examples, Lossy transmission lines ,Smith charts – plotting gamma, High Frequency Amplifier Design, Bandwidth estimation using open-circuit time constants , Bandwidth estimation using short-circuit time constants

Unit III:

Risetime, delay and bandwidth, Zeros to enhance bandwidth, Shunt-series amplifiers, tuned amplifiers Cascaded amplifiers Noise Thermal noise, flicker noise review, Noise figure, LNA Design

Unit IV:

Intrinsic MOS noise parameters ,Power match versus noise match, Large signal performance, design examples & Multiplier based mixers, Mixer Design, Subsampling mixers, RF Power Amplifiers, Class A,AB,B, C amplifiers, Class D,E, F amplifiers, RF Power amplifier design examples

Unit V:

Voltage controlled oscillators, Resonators , Negative resistance oscillators , Phase locked loops Linearized PLL models , Phase detectors, charge pumps, Loop filters, PLL design examples, Frequency synthesis and oscillator Frequency division, integer-N synthesis , Fractional frequency synthesis, Phase noise, General considerations , Circuit examples, Radio Architectures, GSM radio architectures, CDMA, UMTS radio architectures

Suggested Readings:

1. The Design of CMOS Radio-Frequency Integrated Circuits by Thomas H. Lee. Cambridge University Press, 2004.

2. RF Microelectronics by BehzadRazavi.Prentice Hall, 1997.

16EC C204

Embeded Processors and Architecture

Instruction	4 Hours per week	End Exam- Duration	3 Hours
Sessionals	30 Marks	End Exam- Marks	70 Marks

UNIT I

Introduction to DSP Processors: Differences between DSP and other μp architectures, their comparison and need for special ASP^s , RISC & CISC CPUs. Number formats- Fixed point and Floating point formats, Dynamic range and precision.

UNIT II

Data Paths, Basic architectural features, DSP computational building blocks, Bus and Memory architecture, Address generation unit, speed issues, Synchronous serial interface, Multichannel Buffered serial port(McBSP).

UNIT III

Overview of DSP processor design: fixed point DSP^s – Architecture of TMS 320C 54X Processor , addressing modes, Assembly instructions, Pipelining and on-chip peripherals.

UNIT IV

DSP interfacing & software development tools: Interfacing memory and parallel I/O peripherals, DSP tools – Assembler, debugger, c-compiler, linker, editor, code composer studio.

UNIT V

ARM Processor families, Architecture-revisions, Registers, pipeline, exception, interrupts and the vector table; core extensions, introduction to ARM instruction set

Suggested Readings:

1. Avatar Singh and S. Srinivasan, " Digital Signal Processing Implementations Using DSP Microprocessors", Thomson Brooks, 2004.
2. Phil Lapsley, Jeff Bier, AmithShoham and Edward A Lee, "DSP Processor Fundamentals", S. Chand & Company Ltd, 2000.
3. B. Ventakaramani, M. Bhaskar, "Digital Signal Processes, Architecture Processing and Applications", Tata McGraw Hill, 2002.
4. Andrew N.SLOSS, DomonicSymes, Chris Wright "ARM System Developers Guide-Desisning and optimizing system software" ELSEVIER 1st Edition 2004.

16EC C205

Analog and Mixed Signal IC Design

Instruction	4 Hours per week	End Exam- Duration	3 Hours
Sessionals	30 Marks	End Exam- Marks	70 Marks

UNIT I

Brief Review of Small Signal and Large Signal Model of BJTs and MOSFETs.

Current Mirrors and Single Stage Amplifiers – Simple CMOS current mirror, common source amplifier, source follower, common gate amplifier, cascode amplifiers. Source degenerated current mirrors. High out impedance – current mirrors, cascode gain stage Wilson current mirror, MOS differential pair and gain stage. Bipolar current mirrors – bipolar gain stages. Differential pairs with current mirror loads MOS and bipolar widlar current sources,

UNIT II

Operational amplifiers, Basic two stage MOS Operational amplifier–Characteristic parameters, two stage MOS Op-Amp with Cascodes. MOS Telescopic-cascode Op-Amp.MOS Folded cascode op-amp.MOS Active Cascode Op-Amp.Fully differential folded cascode op-amp.Current feedback op-amps.Stability and frequency compensation of op-amps. Phase margin and noise in op-amps.

UNIT – III

Comparators: Op-Amp Based Comparators, Charge Injection Errors – Latched Comparators – CMOS and BiCMOS Comparators – Bipolar Comparators.

Switched capacitor circuits: Basic building blocks; basic operation and analysis, inverting and non inverting integrators, signal flow diagrams, first order filter.

Sample and hold circuits - Performance requirements, MOS sample and hold basics, clock feed through problems,

UNIT – IV

S/H using transmission gates, high input impedance S/H circuits, improved S/H circuits from the point of slewing time, clock feed through cancellations. Data converter fundamentals - performance characteristics, ideal D/A and A/D converters, quantization noise. Nyquist rate D/A converters – decoder based converter, binary-scaled converters.Thermometer code converters, current mode converters.

UNIT – V

Nyquist rate A/D Converters: Integrated converters – successive approximation converters, cyclic A/D converters, Flash or parallel converters, Two step A/D converters, pipelined A/D converters.

Over sampling converters. Over sampling without noise shaping over sampling and with noise shaping, system architecture – digital decimation filters.

supply insensitive biasing, temperature insensitive biasing, band gap reference, band gap reference circuits.

Suggested Readings:

1. Paul.R. Gray & Robert G. Major, Analysis and Design of Analog Integrated Circuits, John Wiley & sons. 2004
2. David Johns, Ken Martin, Analog Integrated Circuit Design, John Wiley & sons. 2004
3. BehzadRazavi, Design of Analog CMOS Integrated Circuits, Tata McGrah Hill. 2002
4. Jacob Baker.R.et.al., CMOS Circuit Design, IEEE Press, Prentice Hall, India, 2000.

16EC C206

Real Time Operating Systems

Instruction	4 Hours per week	End Exam- Duration	3 Hours
Sessionals	30 Marks	End Exam- Marks	70 Marks

UNIT I

Brief Review of Unix Operating Systems (Unix Kernel – File system, Concepts of – Process, Concurrent Execution & Interrupts. Process Management – forks & execution. Programming with system calls, Process Scheduling. Shell programming and filters).

Portable Operating System Interface (POSIX) – IEEE Standard 1003.13 & POSIX real time profile. POSIX versus traditional Unix signals, overheads and timing predictability.

UNIT II

Hard versus Soft Real-time systems – examples, Jobs & Processors, Hard and Soft timing constraints, Hard Real-time systems, Soft Real-time systems. Classical Uniprocessor Scheduling Algorithms – RMS, Preemptive EDF, Allowing for Preemptive and Exclusion Condition.

UNIT III

Concept of Embedded Operating Systems, Differences between Traditional OS and RTOS. Real-time System Concepts, RTOS Kernel & Issues in Multitasking – Task Assignment, Task Priorities, Scheduling, Intertask Communication & Synchronization – Definition of Context Switching, Foreground ISRs and Background Tasks. Critical Section – Reentrant Functions, Interprocess Communication (IPC) – IPC through Semaphores, Mutex, Mailboxes, Message Queues or Pipes and Event Flags.

UNIT IV

VxWorks – POSIX Real Time Extensions, timeout features, Task Creation, Semaphores (Binary, Counting), Mutex, Mailbox, Message Queues, Memory Management – Virtual to Physical Address Mapping.

UNIT V

Debugging Tools and Cross Development Environment – Software Logic Analyzers, ICEs.

Comparison of RTOS – VxWorks, µC/OS-II and RT Linux for Embedded Applications.

Suggested Readings:

1. Jane W.S.Liu, Real Time Systems, Pearson Education, Asia, 2001.
2. Betcnhof, D.R., Programming with POSIX threads, Addison - Wesley Longman, 1997.
3. Wind River Systems, VxWorks Programmers Guide, Wind River Systems Inc.1997.
4. Jean.J.Labrosse, MicroC/OS-II, The CMP Books.
5. Real Time Systems, C.M.Krishna and G.Shin, McGraw-Hill Companies Inc., McGraw Hill International Editions, 1997.

16EC C207

Lab-1 Design and Simulation Laboratory-I

Instruction	3 Hours per week	End Exam- Duration	-
Sessionals	50 Marks	End Exam- Marks	-

Note: all the experiments are to be carried out independently by each student with different specifications. At least 12 experiments are to be carried out.

(i) Design and simulation of combinational circuits

(ii) Design and simulation of sequential circuits

(iii) Design and simulation of mixed signal circuits

(iv) Microcontroller programming

a. Toggling the LEDs,

b. serial data transmission,

c. LCD and Key pad interface

16EC C208

Lab 2 Design and Simulation Laboratory-II

(Synthesis, Backend and Embedded Systems Laboratory)

Instruction	3 Hours per week	End Exam- Duration	-
Sessionals	50 Marks	End Exam- Marks	-

Note: all the experiments are to be carried out independently by each student with different specifications. Atleast 12 experiments are to be carried out.

(i) Synthesis of combinational circuits (4 to 6 MSI digital blocks).

(ii) Synthesis of sequential circuits (4 to 6 MSI digital blocks).

(iii) Schematic simulation, layout, DRC, LVS, parasitic extraction for cells (inverter, NAND gate, NOR gates).

(iv) Programming using real time operating systems

a. Multi tasking using round robin scheduling
b. IPC using message queues
c. IPC using semaphore
d. IPC using mail box

16EC C209

Seminar – 1

Instruction	3 Hours per week	End Exam- Duration	-
Sessionals	50 Marks	End Exam- Marks	-

Prerequisites: A prior knowledge of any Subject in Embedded System and VLSI Design (related to the seminar topic) is required.

Course Objectives:

1. Awareness of how to use values in improving own professionalism
2. Learning about personal and communication styles
3. Learning management of values for personal and business development
4. Increase knowledge of Emotional Intelligence

Oral presentation and technical report writing are two important aspect of engineering education. The objective of the seminar is to prepare the student for a systematic and independent study of the state of the art topics in the advanced fields of Embedded System and VLSI Design and related topics.

Seminar topics may be chosen by the students with advice from the faculty members. Students are to be exposed to the following aspects for a seminar presentation.

- Literature survey
- Organization of the material
- Presentation of OHP slides / LCD presentation
- Technical writing

Each student required to:

1. Submit a one page synopsis before the seminar talk for display on the notice board.
2. Give a 20 minutes time for presentation following by a 10 minutes discussion.
3. Submit a detailed technical report on the seminar topic with list of references and slides used.

Seminars are to be scheduled from the 3rd week to the last week of the semester and any change in schedule shall not be entertained.

For award of sessional marks, students are to be judged by at least two faculty members on the basis of an oral and technical report preparation as well as their involvement in the discussions.

Course Outcomes:

Upon completion of this course, the student will be able to

1. Develop and support a relevant and informed thesis, or point of view, that is appropriate for its audience, purpose, discipline, and theme.
2. Demonstrate effective writing skills and processes by employing the rhetorical techniques of academic writing, including invention, research, critical analysis and evaluation, and revision.
3. Effectively incorporate and document appropriate sources in accordance with the formatting style proper for the discipline and effectively utilize the conventions of standard written English.
4. Better understand the role that effective presentations have in public/professional contexts and gain experience in formal/informal presentation.
5. Identify and critically evaluate the quality of claims, explanation, support, and delivery in public and professional discourse, and understand the factors influencing a speaker's credibility.
6. Develop audience-centered presentations meeting concrete professional objectives and integrating ethical and legal visual aids.
7. Deliver well-rehearsed and polished presentations meeting time, content, and interactive requirements.

16EC C210

SEMINAR - 2

Instruction	3 Hours per week	End Exam- Duration	-
Sessionals	50 Marks	End Exam- Marks	-

Prerequisites: A prior knowledge of any Subject in Embedded System and VLSI Design (related to the seminar topic) is required.

Course Objectives:

1. Awareness of how to use values in improving own professionalism
2. Learning about personal and communication styles
3. Learning management of values for personal and business development
4. Increase knowledge of Emotional Intelligence

Oral presentation and technical report writing are two important aspect of engineering education. The objective of the seminar is to prepare the student for a systematic and independent study of the state of the art topics in the advanced fields of Embedded System and VLSI Design and related topics.

Seminar topics may be chosen by the students with advice from the faculty members. Students are to be exposed to the following aspects for a seminar presentation.

- Literature survey
- Organization of the material
- Presentation of OHP slides / LCD presentation
- Technical writing

Each student required to:

1. Submit a one page synopsis before the seminar talk for display on the notice board.
2. Give a 20 minutes time for presentation following by a 10 minutes discussion.
3. Submit a detailed technical report on the seminar topic with list of references and slides used.

Seminars are to be scheduled from the 3rd week to the last week of the semester and any change in schedule shall not be entertained.

For award of sessional marks, students are to be judged by at least two faculty members on the basis of an oral and technical report preparation as well as their involvement in the discussions.

Course Outcomes:

Upon completion of this course, the student will be able to

1. Develop and support a relevant and informed thesis, or point of view, that is appropriate for its audience, purpose, discipline, and theme.
2. Demonstrate effective writing skills and processes by employing the rhetorical techniques of academic writing, including invention, research, critical analysis and evaluation, and revision.
3. Effectively incorporate and document appropriate sources in accordance with the formatting style proper for the discipline and effectively utilize the conventions of standard written English.
4. Better understand the role that effective presentations have in public/professional contexts and gain experience in formal/informal presentation.
5. Identify and critically evaluate the quality of claims, explanation, support, and delivery in public and professional discourse, and understand the factors influencing a speaker's credibility.
6. Develop audience-centered presentations meeting concrete professional objectives and integrating ethical and legal visual aids.
7. Deliver well-rehearsed and polished presentations meeting time, content, and interactive requirements.

16EC C213

Project work -Project Seminar

Instruction	--------	End Exam- Duration	-
Sessionals	100 Marks	End Exam- Marks	-

Prerequisites: A prior knowledge of subjects related to the project work is required.

Course Objectives:

The overall objective of the project seminar is to help develop an emerging field at the intersection of multi-disciplinary understandings of engineering education

1. To prepare the students for the dissertation to be executed in IV semester, solving a real life problem should be focus of Post Graduate dissertation
2. To explore new research from a range of academic disciplines which throws light on the questions unanswered.
3. To showcase cutting edge research on engineering from outstanding academic researchers.

The main objective of the Project Seminar is to prepare the students for the dissertation to be executed in IV semester. Solving a real life problem should be focus of Post Graduate dissertation. Faculty members should prepare the project briefs (giving scope and reference) at the beginning of the III semester, which should be made available to the students at the departmental library. The project may be classified as hardware / software / modeling / simulation. It may comprise any elements such as analysis, synthesis and design.

The department will appoint a project coordinator who will coordinate the following:

- Allotment of projects and project guides.
- Conduct project - seminars.

Each student must be directed to decide on the following aspects

- Title of the dissertation work.
- Organization.

- Internal / External guide.
- Collection of literature related to the dissertation work.

Each student must present a seminar based on the above aspects as per the following guidelines:

1. Submit a one page synopsis before the seminar talk for display on the notice board.
2. Give a 20 minutes presentation through OHP, PC followed by a 10 minutes discussion.
3. Submit a report on the seminar presented giving the list of references.

Project Seminars are to be scheduled from the 3rd week to the last week of the semester. The internal marks will be awarded based on preparation, presentation and participation.

Course Outcomes:

Upon completion of this course, the student will be able to

1. Develop and support a relevant and informed thesis, or point of view, that is appropriate for its audience, purpose, discipline, and theme.
2. Demonstrate effective writing skills and processes by employing the rhetorical techniques of academic writing, including invention, research, critical analysis and evaluation, and revision.
3. Effectively incorporate and document appropriate sources in accordance with the formatting style proper for the discipline and effectively utilize the conventions of standard written English.
4. Better understand the role that effective presentations have in public/professional contexts and gain experience in formal/informal presentation.
5. Identify and critically evaluate the quality of claims, explanation, support, and delivery in public and professional discourse, and understand the factors influencing a speaker's credibility.
6. Develop audience-centered presentations meeting concrete professional objectives and integrating ethical and legal visual aids.

Deliver well-rehearsed and polished presentations meeting time, content, and interactive requirements.

16EC C214

Project work and Dissertation

Instruction	--	End Exam- Duration	--
Sessionals	100	End Exam- Marks	100

Prerequisites: A prior knowledge of subjects related to the project work is required.

Course Objectives:

The Objectives of the dissertation are to:

1. Put into practice theories and concepts learned on the programme
2. Provide an opportunity to study a particular topic in depth;
3. Show evidence of independent investigation;
4. Combine relevant theories and suggest alternatives;
5. Enable interaction with practitioners (where appropriate to the chosen topic);
6. Show evidence of ability to plan and manage a project within deadlines

The students must be given clear guidelines to execute and complete the project on which they have delivered a seminar in the III semester of the course.

All projects will be monitored at least twice in a semester through student's presentation. Sessional marks should be based on the grades/marks, awarded by a monitoring committee of faculty members as also marks given by the supervisor.

Efforts be made that some of the projects are carries out in industries with the help of industry coordinates.

Common norms will be established for documentation of the project report by the respective department.

The final project reports must be submitted two weeks before the last working day of the semester.

The project works must be evaluated by an external examiner and based on his comments a viva voice will be conducted by the departmental committee containing of HOD, two senior faculty and supervisor.

Course Outcomes:

On satisfying the requirements of this course, students will have the knowledge and skills to:

1. Plan, and engage in, an independent and sustained critical investigation and evaluation of a chosen research topic relevant to environment and society
2. Systematically identify relevant theory and concepts, relate these to appropriate methodologies and evidence, apply appropriate techniques and draw appropriate conclusions
3. Engage in systematic discovery and critical review of appropriate and relevant information sources
4. Appropriately apply qualitative and/or quantitative evaluation processes to original data\
5. Understand and apply ethical standards of conduct in the collection and evaluation of data and other resources
6. Define, design and deliver an academically rigorous piece of research;
7. Understand the relationships between the theoretical concepts taught in class and their application in specific situations
8. Show evidence of a critical and holistic knowledge and have a deeper understanding of their chosen subject area
9. Appreciate practical implications and constraints of the specialist subject

16EC E215Computer Communication Networks

Instruction	3 Hours per week	End Exam- Duration	3 Hours
Sessionals	30 Marks	End Exam- Marks	70 Marks

UNIT – I

Data Communications Model, communication Tasks, basic concepts of Networking and Switching, Line/Networking configurations; Protocols, PDU, OSI and TCP/IP Architectures, Comparisons between OSI and TCP/IP;

UNIT – II

Flow Control, Sliding Window Flow Control, Error control, ARQ Protocols. Data Link Control, Bit stuffing, HDLC frame format, HDLC Modes and Operation; Circuit Switching concepts, Circuit SwitchElements, Three Stage Blocking type Space Division Switch**;**

UNIT – III

Packet Switching, Datagram and Virtual Circuit switching Principles, Effects of variable packet size. Control Signaling Functions, In Channel Signaling, Common Channel Signaling, Introduction to Signaling System Number 7 (SS7); Topologies, Choice of Topology, Ring and Star Usage, MAC and LLC, Generic MAC Frame Format; Hubs, Switches.Bridge, Bridge Operation, Bridges and LANs.

UNIT – IV

Routing, Routing strategies; Internetworking; Internet Protocol, IP address, IPv4, IPv6 comparison; Transport layer protocols, UDP Operation, TCP features, TCP/IP Addressing Concepts, Credit based Flow Control, Congestion Control.

UNIT – V

Wireless LAN, IEEE 802.11 Architecture, IEEE 802.11- Medium Access Control logic; ATM, features of ATM, Quality of Service in ATM; Security in the Internet Network Management System, SNMP.

Suggested Readings:

1) William Stallings, “Data and Computer Communications”, Ninth Edition, Pearson Prentice Hall, 2011.
2) Behrouz A. Forouzan, “Data Communications and Networking”, Fourth Edition, Tata McGraw Hill, 2007.

16EC E216

Embedded System Design

Instruction	3 Hours per week	End Exam- Duration	3 Hours
Sessionals	30 Marks	End Exam- Marks	70 Marks

UNIT – I

Introduction to Embedded Systems: An Embedded system, Classification, processor in the system, other hardware units, structural units in a processor, processor selection for an embedded system, memory devices, memory selection for an embedded system, introduction to ARM processors.

UNIT – II

Devices and Buses: I/O devices, Serial communication using IIC and CAN buses, advanced I/O buses between the networked multiple Devices, Device drivers: Classification, Parallel port device drivers in a system, Serial port device drivers in a system.

UNIT – III

Interprocess communication and synchronization of processes, Task and Threads: Multiple processes in an application, problem of sharing data by multiple tasks and routines, Embedded programming in C++ and Java.

UNIT – IV

Real time Operating Systems: Operating system services, Real time operating system services, interrupt routines in RTOS Environment, RTOS Task scheduling, embedded Linux internals, OS Security issues, Mobile OS.

UNIT – V

Hardware-Software Co-Design in an Embedded System: Embedded system project Management, Embedded system Design and Co-Design issues in system development process. Design cycle in system development phase for an embedded system, Emulator and ICE, Use of software tools for development of Embedded systems, Case studies of programming with RTOS(Examples: Automatic chocolate vending machine, vehicle tracking system, Smart card).

Suggested Readings:

1. Raj Kamal,"Embedded Systems" Architecture, Programming and Design, TMH, 2006.
2. Jonathan W Valvano, "Embedded Micro Computer Systems" Real Time Interfacing, Books / cole, Thomson learning 2006.
3. Arnold S Burger, "Embedded System Design" An Introduction to Processes, Tools and Techniques by CMP books, 2007.
4. David.E. Simon, "An Embedded Software Primer", Pearson Edition, 2009.
5. Andrew N.sloss, Dominic Symes, Chris Wright, "ARM System Developer's guide", Elsevier publications 2005.

16EC E217

Advanced Computer Organization

Instruction	3 Hours per week	End Exam- Duration	3 Hours

Sessionals	30 Marks	End Exam- Marks	70 Marks

UNIT – I:

Processor Design: CPU Organization, Data Representation, Instruction Formats, Data Path Design: Fixed Point Arithmetic and Floating Point Arithmetic, Instruction Pipelining, Super Scalar techniques, Linear pipeline processors, Super scalar and super pipeline design, Multi vector and SIMD computers.

UNIT – II:

Control Unit Design:

Basic Concepts: Hardwired Control Unit Design approach, Micro-programmed Control Unit Design Approach, Micro program sequencer, Case studies based on both the approaches.

UNIT – III:

Memory Organization:

Internal memory, computer memory system overview, The memory Hierarchy, Random access memories, Cache memory, Elements of cache design, Virtual memory- protection and examples of virtual memory, Replacement Policies.

UNIT – IV:

I-**O Organization**: Accessing I/O Devices, Programmed I-O, Interrupts, DMA, Bus Arbitration; Synchronous bus and asynchronous bus, Interface circuits, Parallel port, Serial port, standard I/O interfaces, IO Processor, PCI bus, SCSI bus, USB bus protocols.

UNIT – V:

Parallel Computer Systems:

Instruction Level Parallelism (ILP) – Concept and Challenges, Dynamic Scheduling, Limitations on ILP, Thread Level Parallelism, Multi-processors – Characteristics, Symmetric and Distributive Shared Memory Architecture, Vector Processors and Super computers.

Suggested Readings:

1. William Stallings, Computer Organization and Architecture designing for Performance, 7th edition, PHI, 2007.
2. Carl Hamacher, Vranesic, Zaky, Computer Organization, 5th edition, MGH.
3. Hayes John P; Computer Architecture and organization; 3rd Edition, MGH, 1998.
4. John L. Hennessy and David A. Patterson, Computer Architecture – A quantitative Approach, 3rd Edition, Elsevier, 2005.

16EC E218

CPLD & FPGA Architectures and Applications

Instruction	3 Hours per week	End Exam- Duration	3 Hours
Sessionals	30 Marks	End Exam- Marks	70 Marks

UNIT I

Programmable logic: Programmable read only memory (prom), programmable logic array (pla), programmable array logic (pal). Sequential programmable logic devices (splds). Programmable gate arrays (pgas), CPLD and FPGA, design flow using FPGA, programming technologies.

UNIT II

FPGAs: Field Programmable Gate Arrays – Logic blocks, routing architecture, Logic cells and features of commercially available FPGA's- XILINX XC4000, virtexII FPGA's, XILINX SPARTAN II, Alteras Act1, Act2, Act3 FPGA's, Actel FPGA's, AMD FPGA.

UNIT III

CPLD's: complex programmable logic devices, logic block, I/O block, interconnect matrix, logic blocks and features of altera flex logic 10000 series CPLD's , max 7000 series CPLD's, AT & T – ORCA's (Optimized Reconfigurable Cell Array), cypres flash 370 device technology, lattice plsi's architectures.

UNIT IV

Placement: objectives, placement algorithms: Mincut-Based placement, iterative improvement placement,simulated annealing.

Routing: objectives, segmented channel routing, Maze routing, Routability estimation, Net delays, computing signal delay in RC tree networks.

UNIT V

Digital Front End and back End tools for FPGAs & ASICs, FPGA implementation steps.

Verification: introduction, logic simulation, design validation, timing verification.

Testing concepts: failures, mechanisms and faults, fault coverage, ATPG methods, programmability failures.

Suggested Reading:

1. P.K. Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, Pearson Education 2009.
2. S. Trimberger, Edr., Field Programmable Gate Array Technology, Kluwer Academic Publications, 1994.

3. J. Old Field, R. Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, 1995.
4. S. Brown, R. Francis, J. Rose, Z.Vransic, Field Programmable Gate array, Kluwer Publn, 1992.
5. Manuals from Xilinx, Altera, AMD, Actel.

16EC E219

Design for Testability

Instruction	3 Hours per week	End Exam- Duration	3 Hours
Sessionals	30 Marks	End Exam- Marks	70 Marks

UNIT I

Introduction to Test and Design fro Testability (DFT) Fundamentals.

Modeling: Modeling digital circuits at logic level, register level and structural models. Levels of modeling.

Logic Simulation: Types of simulation, Delay models, Element evaluation, Hazard detection, Gate level event driven simulation.

UNIT II

Fault Modeling – Logic fault models, Fault detection and redundancy, Fault equivalence and fault location. Single stuck and multiple stuck – Fault models. Fault simulation applications, General techniques for Combinational circuits.

UNIT III

Testing for single stuck faults (SSF) – Automated test pattern generation (ATPG/ATG) for SSFs in combinational and sequential circuits, Functional testing with specific fault models.Vector simulation – ATPG vectors, formats, Compaction and compression, Selecting ATPG Tool.

UNIT IV

Design for testability – testability trade-offs, techniques. Scan architectures and testing – controllability and absorbability, generic boundary scan, full integrated scan, storage cells for scan design. Board level and system level DFT approaches. Boundary scan standards. Compression techniques – different techniques, syndrome test and signature analysis.

UNIT V

Built-in self-test (BIST) – BIST Concepts and test pattern generation.Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief ideas on some advanced BIST concepts and design for self-test at board level. Memory BIST (MBIST): Memory test architectures and techniques – Introduction to memory test, Types of memories and integration, Embedded memory testing model. Memory test requirements for MBIST.Brief ideas on embedded core testing.

Suggesting Readings:

1. MironAbramovici, Melvin A. Breur, Arthur D. Friedman, Digital Systems Testing and Testable Design, Jaico Publishing House, 2001.
2. Alfred Crouch., Design for Test for Digital ICs & Embedded Core Systems, Prentice Hall.
3. Robert J. Feugate, Jr., Steven M. Mentyn, Introduction to VLSI Testing, Prentice Hall, Englehood Cliffs, 1998.

16EC E220

VLSI Technology

Instruction	3 Hours per week	End Exam- Duration	3 Hours
Sessionals	30 Marks	End Exam- Marks	70 Marks

UNIT I

Introduction – Integrated Circuits Review of history of VLSI technology progress–. Electronic Functions – Components – Analog and Digital ICs.Basic Devices in ICs – Structures Resistors – Capacitors – Inductors.Diodes – Bipolar Junction Transistors – Field Effect Transistors.Isolation techniques in MOS and bipolar technologies.

UNIT II

Monolithic ICs – Silicon as the Base Material and its advantages, various Layers of ICs – Substrate – Active Layer -Oxide/Nitride Layers – Metal/Poly Silicon Layers – Functions of Each of the Layers. Process Flow for Realization of Devices.Description of Process Flow for Typical Devices viz., FET and BJT.

UNIT III

Silicon Wafer Preparation – Electronic Grade Silicon – CZ and FZ Methods of Single Crystal Growth – Silicon Shaping – Mechanical Operations, Chemical Operations – Prefabrication Processes.

Epitaxy: Growth Dynamics – Process Steps. Vapour phase, Solid phase and Molecular Beam Epitaxial Processes. Epitaxial Reactors.

Oxide Growth: Structure of SiO_2, Growth Mechanism and Dynamics – Oxide Growth by Thermal method.

UNIT IV

Deposition techniques Chemical Vapour Deposition (CVD) and associated methods like LPCVD and PECVD. PVD thermal evaporation and sputtering. Step coverage issues.

Lithography: Steps involved in Photolithography – Quality of the Pattern – photo resists and their characteristics, optical exposure systems contact and projection systems, steppers, X-ray – Electron Beam Lithography.

Etching: Chemical, Electro Chemical – Plasma (Dry Etching) Reactive Plasma Etching.

UNIT V

Ion implantation: Range and Penetration Depth – Damage and Annealing – Ion Implantation machine.Diffusion: Constant and Infinite Source Diffusions – Diffusion Profiles – Diffusion Systems – Multiple Diffusions and Junction Formations. Packaging: die and Bonding and Packaging, Testing.Clean rooms and their importance in VLSI technology

Suggested Reading:

1. S.M. Sze,VLSI Technology, McGrawhill International Editions.
2. CY Chang and S.M. SZe , VLSI Technology, Tata McGraw-Hill Companies Inc.

3. J.D.Plummer, M.D.Deal and P.B.Griffin ,The Silicon VLSI Technology Fundamentals, Practice and modeling, Pearson Education 2009
4. Stephen A, The Science and Engineering of Microelectronic Fabrication , Campbell Oxford 2001

16EC E221

Low Power VLSI Design

Instruction	3 Hours per week	End Exam- Duration	3 Hours
Sessionals	30 Marks	End Exam- Marks	70 Marks

UNIT-I

Introduction and need of low power design, sources of power dissipation, MOS transistor leakage components, SOI technology, FinFET, Back gate FET, power and energy basics, power dissipation in CMOS circuits, Energy-delay product as a metric, design strategies for low power.

UNIT-II

Power Estimation Techniques: Circuit Level – Modeling of Signals, Signal Probability Calculations, Statistical techniques; High Level Power Analysis – RTL Power Estimation, Fast Synthesis, Analytical Approaches, Architectural Power Estimation.

UNIT-III

Power Optimization Techniques – I: Dynamic Power Reduction – Dynamic Power Component, Circuit Parallelization, Voltage Scaling Based Circuit Techniques, Circuit Technology – Independent Power Reduction, Circuit Technology Dependent Power Reduction; Leakage Power Reduction – Leakage Components, Design Time Reduction Techniques, Run-time Stand-by Reduction Techniques, Run-time Active Reduction Techniques Reduction in Cache Memories.

UNIT-IV

Power Optimization Techniques – II: Low Power Very Fast Dynamic Logic Circuits, Low Power Arithmetic Operators, Energy Recovery Circuit Design, Adiabatic – Charging Principle and its implementation issues.

UNIT-V

Software Design for Low Power: Sources of Software Power Dissipation, Software Power Estimation, Software Power Optimizations, Automated Low-Power Code Generation, Co-design for Low Power.

Suggested Readings:

1. Kaushik Roy and Sharat Prasad, Low-Power CMOS VLSI Circuit Design, Wiley Inter-science Publications, 2000.
2. Christian Piguet, Low Power CMOS Circuits Technology, Logic Design and CAD Tools, 1st Indian Reprint, CRC Press, 2010.
3. J. Rabaey,Low Power Design Essentials, 1st Edition, Springer Publications, 2010.

16EC E222

VLSI Signal Processing

Instruction	3 Hours per week	End Exam- Duration	3 Hours
Sessionals	30 Marks	End Exam- Marks	70 Marks

UNIT – I

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms. Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power, Retiming: Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques

UNIT – II

Folding and Unfolding, Folding : Introduction -Folding Transform - Register minimization Techniques – Register minimization in folded architectures – folding of multirate systems, Unfolding: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding

UNIT – III

Systolic Architecture Design: Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays

UNIT – IV

Fast Convolution: Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT – V

Low Power Design: Scaling Vs Power Consumption –Power Analysis, Power Reduction techniques – Power Estimation Approaches, Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing

Suggested Readings:

1. Keshab K. Parthi, VLSI Digital Signal Processing- System Design and Implementation – 1998, Wiley Inter Science.

2. Kung S. Y, H. J. While House, T. Kailath, VLSI and Modern Signal processing, 1985, Prentice Hall.
3. Jose E. France, YannisTsividis, Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing –1994, Prentice Hall.
4. Medisetti V. K ,VLSI Digital Signal Processing , IEEE Press (NY), USA, 1995.

16EC E223

Advanced Digital Design with Verilog HDL

Instruction	3 Hours per week	End Exam- Duration	3 Hours
Sessionals	30 Marks	End Exam- Marks	70 Marks

UNIT-I

Review of Verilog HDL, Modeling styles: Behavioral, Dataflow, and Structural Modeling, gate delays, switch-level Modeling, Hierarchal structural modeling.

UNIT-II

Modeling of basic MSI Combinational Logic modules and Sequential Logic modules.Finite State Machine modeling.

UNIT-III

Design options of Digital Systems, Hierarchical system design, ASIC designs, PLD modeling, CPLD and FPGA devices.

Synthesis: Design flow of ASICs and FPGA based system, design environment and constraints logic synthesizers, Language structure synthesis, coding guidelines for clocks and reset.

UNIT-IV

Verification: Functional verification, simulation types, Test Bench design, Dynamic timing analysis, static timing analysis, value change dump (VCD) files. FPGA based design flow- a case study.

UNIT-V

Design Examples: Adders and Substractors, Multiplicaton and Division Algorithms, ALU, Digital Signal Processing modules: FIR and IIR Filters, Bus structures, Synchronous & Asynchronous data transfer, UART, baud rate generator. A simple CPU design.

Suggested Readings:

1. Ming-Bo Lin., Digital System Designs and Practices Using Verilog HDL and FPGAs. Wiley, 2008.
2. Michael D. Ciletti, Advanced Digital Design with the Verilog HDL", PHI, 2005.
3. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Pearson Education, 2005.

16EC E224

VLSI Physical Design Automation

Instruction	3 Hours per week	End Exam- Duration	3 Hours
Sessionals	30 Marks	End Exam- Marks	70 Marks

UNIT I

Scope of physical design – Components of VLSI – Various layers of VLSI – Typical structures of BJTS, MOSFETS, Resistors, capacitors, inductors, interconnects, brief review of technology, cost and performance analysis.

UNIT II

Basic concepts of Physical Design - layout of basic structures – wells, FET, BJT, resistors, capacitors, contacts, vias and wires (Interconnects). Mask overlays for different structures. Parasitics – latch up and its prevention. Device matching and common centroid techniques for analog circuits

UNIT III

Design rules – fabrication errors, alignment sequence and alignment inaccuracies, process variations and process deltas, drawn and actual dimensions and their effect on design rules– scalable design rules. Scalable CMOS (SCMOS) design rules, layout design, and stick diagrams, Hierarchical stick diagrams.

UNIT IV

Cell concepts – cell based layout design – Wein-berger image array – physical design of logic gates – NOT, NAND and NOR – design hierarchies. System level physical design, large scale physical design, interconnect delay modeling, floor planning, routing and clock distribution.

UNIT V

CAD Tools: Layout editors, Design rule checkers, circuit extractors – Hierarchical circuit extractors – Automatic layout tools, silicon compilers, modeling and extraction of circuit parameters from physical layout.

Suggested Readings:

1. Preas, M. Lorenzatti, "Physical Design and Automation of VLSI Systems", The Benjamin – Cummins Publishers, 1998.
2. M. Shoji, "CMOS Digital Circuit Technology", Prentice Hall, 1987.
3. John P. Uyemura, Introduction to VLSI Circuits and Systems, John Wiley & sons, Inc.
4. Modern VLSI Design (System on Chip), Woyne Wolf, Pearson Education, 2002.
5. R. Jacob Baker; Harry W.Li., David E. Boyce, CMOS Circuit Design, Layout and Simulation, IEEE Press, Prentice Hall of India.

16EC E225

System on Chip Architecture

Instruction	3 Hours per week	End Exam- Duration	3 Hours
Sessionals	30 Marks	End Exam- Marks	70 Marks

UNIT – I

Introduction to Processor Design: Abstraction in Hardware Design, MUO a simple processor , Processor design trade off, Design for low power consumption. ARM Processor as System-on-Chip: Acorn RISC Machine – Architecture inheritance – ARM programming model – ARM development tools – 3 and 5 stage pipeline ARM organization – ARM instruction execution and implementation – ARM Co-processor interface

UNIT – II

ARM Assembly Language Programming: ARM instruction types – data transfer, data processing and control flow instructions – ARM instruction set – Co-processor instructions. Architectural Support for High Level Language: Data types – abstraction in Software design – Expressions – Loops – Functions and Procedures – Conditional Statements – Use of Memory.

UNIT – III

Memory Hierarchy: Memory size and speed – On-chip memory – Caches – Cache design- an example – memory management

UNIT – IV

Architectural Support for System Development: Advanced Microcontroller bus architecture – ARM memory interface – ARM reference peripheral specification – Hardware system prototyping tools – Armulator – Debug architecture

UNIT – V

Architectural Support for Operating System: An introduction to Operating Systems – ARM system control coprocessor – CP15 protection unit registers – ARM protection unit – CP15 MMU registers–ARM MMU Architecture–Synchronization–Context Switching input and output

Suggested Readings:

1. Steve Furber, ARM System on Chip Architecture, 2nd ed., Addison Wesley Professional, 2000.
2. Ricardo Reis, Design of System on a Chip: Devices and Components, 1st ed., Springer, 2004.
3. Jason Andrews, Newnes, Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) , BK and CDROM
4. PrakashRashinkar, System on Chip Verification – Methodologies and Techniques, Peter Paterson and Leena Singh L ,Kluwer Academic Publishers, 2001.

16EC E226

Physics of Semiconductor Devices

Instruction	3 Hours per week	End Exam- Duration	3 Hours
Sessionals	30 Marks	End Exam- Marks	70 Marks

UNIT I

Properties of Semiconductors: Crystal Structure Energy Bands, Carrier Transport Phenomena. (Mobility of Carriers, Resistivity and Hall Effect, Generation – Recombination Processes).High

Field Phenomena.Gunn Effect and Negative Resistance Characteristics.Basic Equation for Describing Current Flow.

UNIT II

Bipolar Devices: Ideal P-N Junctions, V-I Characteristics, Effect of Generation – Recombination Processes. Effect of High Injection.Junction Breakdown, Depletion and Diffusion Capacitance.Hetero Junctions. Bipolar Transistor – Characteristics – Equivalent Circuit - Ebers - Moll Model – Gummel Poon Model, Microwave and High Frequency Transistor Structures – Breakdown of Transistors including Secondary Breakdown.

UNIT III

Field Effect Transistors – JFET, MESFET – Characteristics.

MOSFET and MISFET: MOS Diode – Capacitance Vs Voltage Curves. Interface Trapped Charges – oxide Charge. V-I Characteristics of MIS Diodes with Thin Insulating Films. MOS/MISFET – Different Types – Basic device Characteristics – Sub-threshold Region Characteristics – Buried Channel Devices.

UNIT IV

Short Channel Effects – On sub-threshold Current, On Threshold Voltage – On the Structures – Shallow Junctions – Breakdown Voltage – Band Gap Engineering – Thin Film Transistor – Silicon On Insulator (SOI) Devices.

UNIT V

Floating Gate Devices for Non-volatile Memories. MIOS Devices – Gallium Arsenide Devices – Gunn Devices (or Transferred Electron Devices TEDS) – Functional Devices for Microwave Oscillators.LEDS and Laser Diodes.

Suggested Readings:

1. S.M. Sze, Physics of Semiconductor Devices, John Wiley & Sons, 1981.
2. Dewitt G. ONG., Modern MOS Technology: Processes, Devices and Design,Mc. Graw Hill Book Company. 1984.
3. CHEN , VLSI Hand book, CRC Press, IEEE Press, 2000.

16EC E227

Optimization Techniques

Instruction	3 Hours per week	End Exam- Duration	3 Hours
Sessionals	30 Marks	End Exam- Marks	70 Marks

UNIT I

Use of optimization methods.Introduction to classical optimization techniques, motivation to the simplex method, simplex algorithm, sensitivity analysis.

UNIT II

Search methods - Unrestricted search, exhaustive search, Fibonocci method, Golden section method, Direct search method, Random search methods, Univariate method, simplex method, Pattern search method.

UNIT III

Descent methods, Gradient of function, steepest decent method, conjugate gradient method.

Characteristics of constrained problem, Direct methods, The complex method, cutting plane method.

UNIT IV

Review of a global optimization techniques such as Monte Carlo method, Simulated annealing and Tunneling algorithm.

UNIT V

Generic algorithm - Selection process, Crossover, Mutation, Schema theorem, comparison between binary and floating point implementation.

Suggested Readings:

1. SS Rao, “Optimization techniques”, PHI, 1989.
2. Zhigmiew Michelewicz, “Genetic algorithms + data structures = Evaluation programs”, Springer Verlog - 1992.
3. Merrium C. W., “Optimization theory and the design of feedback control systems”, McGraw Hill, 1964.
4. Weldo D.J., “Optimum seeking method”, PHI, 1964.