

Name of Faculty Dr. Mohd Ziauddin Jahangir
 Designation Assistant Professor
 Nature of Job/Appointment Regular
 Date of Joining 22 - 09 - 2014
 E-mail Jahangir_ece@cbit.ac.in



| Education Qualifications | Name of the Degree | Class |
|--------------------------|--|-------------|
| Ph. D | Doctor of Philosophy (VLSI) | Awarded |
| PG | M. E. (Embedded Systems and VLSI Design) | I |
| UG | B.E. (ECE) | Distinction |

Work Experience

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| Teaching | 10 Years |
| Research | 06 years |
| Industry | 01 year |
| Others | -- |

Area of Specialization

Analog Circuit Design, Analog VLSI Design, Mixed Signal Circuit Design, RF IC Design, Microprocessor and Microcontrollers, Embedded Systems Design, Control Systems, SoC Design.

Professional Memberships

IEEE, IEEE-CASS

Responsibilities held at Institution Level

1. Member, IQAC
2. Member, NIRF Committee.

Responsibilities held at Department Level

1. CO and PO Evaluation
2. NBA-OBE coordinator

Research Guidance

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Awards Received

Best Paper Award for the work on "Development of Ternary SRAM Memory Cell" at IEEE-INCON, 2015. New-Delhi

Courses Handled at Under Graduate / Post Graduate Level.

Analog and Digital CMOS VLSI Design, Analog IC Design, Analog and Mixed Signal Design, System on Chip, Embedded Systems, Analog Circuits, Linear and Digital Integrated Circuits, Microcontrollers, Computer Architecture and Organization, Control Systems

No. of Papers Published

National Journals – -- International Journals – 4 National Conference – 01 International Conference – 08

Projects Carried out

1. Chief Investigator of the Project titled "**The design, fabrication and development of silicon proven IP core for high resolution ADPLL of High Resolution ADPLL IP Core**" sponsored by Ministry of Electronics and Information technology (MeitY) under Chip-2-Startup (C2S) program. Amount **Rs.1.91** Crores.
2. Consultancy project titled "**Study of ultrasound based fluid rate measurement technology**" for SKYLARK Smartmeters Pvt. Ltd. amounting Rs.3.00 Lakhs

Patents

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Technology Transfer

- Ultrasound fluid flow rate measurement technology transfer to SKYLARK Sartmeters
- a. Analog Simulations using CADENCE tools at Osmania University College of Engineering (A), OU, Hyderabad, 2017.

Invited Speaker

No. of Books/Chapter Published with details

- b. Jahangir, Mohd Ziauddin, et al. "Design of an All Digital Phase- Locked Loop Using Cordic Algorithm." Advances in Signal Processing and Communication Engineering: Select Proceedings of ICASPACE 2021. Singapore: Springer Nature Singapore, 2022. 143-149.

Details of Short-Term Training Programs/Faculty Development Programs/Seminars/Workshops. Other -- Trainings (**Attended and/or Organized**).

Details of Journal Publications/ Conferences (**National and International**) **International Conference :**

1. Jahangir, Mohd Ziauddin, and Chandra Sekhar Paidimarry. "Design of a Novel Charge Pump based Current Starved Ring Oscillator with Reduced Phase Noise." 2023 International Conference for Advancement in Technology (ICONAT). IEEE, 2023.
2. Jahangir, Mohd Ziauddin, et al. "Design and Implementation of FPGA based DDS-ADPLL for Resonant Frequency Tracking in Sensors." 2022 IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT). IEEE, 2022.
3. Quadri, Syed Ali Imran, and Mohd Ziauddin Jahangir. "Design, Implementation and Performance Comparison of Different Branch Predictors on Pipelined-CPU." 2017 International Conference on Computer, Electrical & Communication Engineering (ICCECE). IEEE, 2017.
4. Mounika, J., K. Ramanujam, and Mohd Ziauddin Jahangir. "CMOS based design and simulation of ternary full adder and Ternary coded Decimal (TCD) adder circuit." 2016 International Conference on Circuit, Power and Computing Technologies (ICCPCT). IEEE, 2016.
5. Jahangir, Mohd Ziauddin, and K. Venkata Narasimha. "Design of a new ternary SRAM cell (ZV-SRAM) based on innovative level shift based ternary inverter (ZV-Inverter)." 2015 Annual IEEE India Conference (INDICON). IEEE, 2015.
6. Jahangir, Mohd Ziauddin, P. Chandrasekhar, and NV Koteswara Rao. "Design and simulation of programmable band-gap reference circuit." 2015 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia). IEEE, 2015.
7. Jahangir, Mohd Ziauddin, and Chandra Sekhar Paidimarry. "Design of programmable Op-Amps with minimized DC variations at output." 2013 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia). IEEE, 2013.

National /International Journal :

1. Jahangir, Mohd Ziauddin, and Paidimarry Chandra Sekhar. "Design of novel hybrid-digitally controlled oscillator for ADPLL." Memories-Materials, Devices, Circuits and Systems (2023): 100052. Elsevier
2. Jahangir, Mohd Ziauddin, and J. Mounika. "Design and simulation of an innovative CMOS ternary 3 to 1 multiplexer and the design of ternary half adder using ternary 3 to 1 multiplexer." Microelectronics Journal 90 (2019): 82-87. Elsevier.
3. Jahangir, Mohd Ziauddin, et al. "Design of an All Digital Phase-Locked Loop Using Cordic Algorithm." Advances in Signal Processing and Communication Engineering: Select Proceedings of ICASPACE 2021. Singapore: Springer Nature Singapore, 2022. 143-149.
4. Jahangir, Mohd Ziauddin and Paidimarry Chandra Sekhar. " The Design of DDS ADPLL using ARM Micro Controller." IJRASET 2022.