

Name of the Department: Electronics and Communication Engineering

Academic Year: 2020-21(2021 Passed Out)

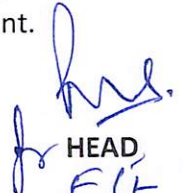
PG Program: ES & VLSID

	Target Fixed	Target Achieved	Observation(Attained/Not Attained)	Actions Taken		
				A1	A2	A3
PO1	2.10	2.18	Attained	--	--	--
PO2	2.10	2.10	Attained	--	--	--
PO3	2.10	2.14	Attained	--	--	--
PO4	2.10	2.22	Attained	--	--	--
PO5	2.10	2.18	Attained	--	--	--

**Evidences:**

1. Drive Link for CO PO mapping Sheets Semester wise: [https://sites.google.com/a/cbit.ac.in/cbit\\_ece\\_obe/home](https://sites.google.com/a/cbit.ac.in/cbit_ece_obe/home)
2. Complete PO attainment table for 2017 batch (AY: 2020-21) hard copy endorsed by head of the department.

  
In-Charge

  
HEAD  
ECE  
HEAD  
DEPARTMENT OF ECE  
Chaitanya Bharathi Institute of Technology  
Hyderabad-500 075

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S.No	Course	PO-1	PO-2	PO-3	PO-4	PO-5
1	Analog and Digital CMOS VLSI Design	1.712	1.775	1.39	1.6525	1.6525
2	Microcontrollers and Programmable Digital Signal Processors	1.624	1.6	1.605714286	1.52	1.651428571
3	Research Methodology and IPR	1.896	1.896	1.896	1.896	1.896
4	Advanced computer orgazniation	1.426153846	1.385714286	1.416	1.29	1.436
5	VLSI Technology and Physical Design Automation	1.772	1.11	1.9375	-	-
6	English for Research Paper Writing	-	-	2.28	2.28	2.28
7	Analog and Digital CMOS VLSI Design Lab	1	1	-	1	-
8	Microcontrollers and Programmable Digital Signal Processors Lab	1.4	1.4	1.4	1.4	1.4
9	Embedded System Design using RTOS	2.088	2.18	2.04	2.712	-
10	VLSI Design Verification and Testing	1.754	1.514444444	1.646666667	1.74	1.716666667
11	Low Power VLSI Design	1.656	1.7925	1.565	1.5	-
12	SoC Design	0.746	0.739	0.73	0.7975	0.7975
13	Value Education	-	-	2.28	2.28	2.28
14	RTL Simulation and Synthesis with PLDs Lab	3	3	-	3	-
15	RTOS and VLSI Design Verification Lab	3	3	-	3	-
16	Mini Project with Seminar	3	-	3	3	3
17	CPLD&FPGA (Program Elective)	2.322857143	2.301818182	2.177142857	2.291428571	2.274285714
18	Cost Management of Engineering Projects(open elective)	-	-	2.088	2.088	2.088
19	Dissertation /Phase-I	3	3	3	3	3
20	Dissertation /Phase-II	2.333333333	2.2	2.25	2.2	2.2
	PO-Attainment	1.98	1.87	1.92	2.03	1.98

	PO1	PO2	PO3	PO4	PO5
PO-DIRECT-Attained	1.98	1.87	1.92	2.03	1.98
PO-INDIRECT-Attained	3.00	3.00	3.00	3.00	3.00
<b>FINAL-PO/PSO-Attained</b>	2.18	2.1	2.14	2.22	2.18
PO Mapping Max	2.55	2.33	2.03	2.19	2.29
PO Indirect Max	3.00	3.00	3.00	3.00	3.00
PO MAX	2.64	2.46	2.22	2.35	2.43
0.7					
Target (70% of MAX)	2.1	2.1	2.1	2.1	2.1
Result	Attained	Attained	Attained	Attained	Attained
Attained %	82.58	85.37	96.4	94.47	89.71