

**AY 2018-19**  
**SCIE**

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2. **Mohd Ziauddin Jahangir , J. Mounika,Design** and simulation of an innovative CMOS ternary 3 to 1 multiplexer and the design of ternary half adder using ternary 3 to 1 multiplexer, Microelectronics Journal, ELSEVIER, <https://doi.org/10.1016/j.mejo.2019.05.007>, 14th may 2019.