Scheme of Instruction and Syllabi

of

ME I to IV SEMESTERS

of

TWO YEAR PG COURSE

in

EMBEDDED SYSTEMS & VLSI DESIGN

(AICTE Model Curriculum with effect from AY 2020-21)

CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY

(Autonomous Institution under UGC, Affiliated to Osmania University)
Department of Electronics &Communication Engineering
Accredited by NBA and NAAC-UGC,
Chaitanya Bharathi (Post), Gandipet, Hyderabad–500075

CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY (A)

OUR MOTTO: SWAYAM TEJASWIN BHAVA

VISION and MISSION of the INSTITUTE

Vision

To be a centre of excellence in technical education and research.

Mission

To address the emerging needs through quality technical education and advanced research.

VISION and MISSION of DEPT. of ECE

Vision

To develop the department into a full-fledged center of learning in various fields of Electronics & Communication Engineering, keeping in view the latest developments.

Mission

To impart value based technical education and train students and to turn out full pledged engineers in the field of Electronics & Communication Engineering with and overall background suitable for making a successful career either in industry/research or higher education in India/Abroad.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Program Educational Objectives of M.E (Embedded Systems and VLSI Design) Programme

PEO1	Graduates will apply engineering expertise to solve real world problems in the areas of Embedded Systems and VLSI Design
PEO2	Graduates will have the ability to adopt latest technologies
PEO3	Graduates will be able to carry out research in the fields of Micro Electronics and Embedded Systems
PEO4	Graduates will develop professional ethics, effective communication skills, self-confidence and societal responsibilities

Program Outcomes of M.E (Embedded Systems and VLSI Design) Programme

PO1	Students will be able to analyze, implement and demonstrate the Embedded Systems and Electronics System Designs
PO2	Students will be able to use modern engineering tools/software to Design and Develop the Embedded Systems and also both the Analog and Digital VLSI Systems
PO3:	Students will be able to write and present substantial technical report/document
PO4	Students will able to independently carry out research/investigation and development work in the domain of ES&VLSI Design
PO5	Students will be able to develop self-confidence, team work, skills for lifelong learning and committed to social responsibilities

CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY (A)

(AICTE Model Curriculum with effect from AY 2020-20)

M.E (Embedded Systems & VLSI Design)

SEMESTER – I

S.No	Course Code	Title of the Course	Scheme of Instruction			Scheme of Examination			Credits
			Hours per week			Duration of SEE in Hours	Maximum Marks		
			L	T	P		CIE	SEE	
THEORY									
1	20ECC201	Analog and Digital CMOS VLSI Design	3	--	--	3	40	60	3
2	20ECC203	Microcontrollers and Programmable Digital Signal Processors	3	--	--	3	40	60	3
3		Program Elective-I	3	--	--	3	40	60	3
4		Program Elective-II	3	--	--	3	40	60	3
5	20ME C103	Research Methodology and IPR	2	--	--	2	25	50	2
6		Audit Course-I	2	--	--	2	--	50	Non-Credit
PRACTICALS									
7	20ECC205	Analog and Digital CMOS VLSI Design Lab	--	--	4	--	50	--	2
8	20ECC206	Microcontrollers and Programmable Digital Signal Processors Lab	--	--	4	--	50	--	2
Total			**16**	**--**	**8**	**--**	**285**	**340**	**18**
Clock Hours Per Week: 24									

L: Lecture **D: Drawing** **CIE: Continuous Internal Evaluation**

T: Tutorial **P: Practical/Mini Project with Seminar/ Dissertation Phase** **SEE: Semester End Examination**

CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY (A)

(AICTE Model Curriculum with effect from AY 2020-20)

M.E (Embedded Systems & VLSI Design)

SEMESTER – II

S.No	Course Code	Title of the Course	Scheme of Instruction			Scheme of Examination			Credits
			Hours per week			Duration of SEE in Hours	Maximum Marks		
			L	T	P		CIE	SEE	
THEORY									
1	20ECC202	Embedded System Design Using RTOS	3	--	--	3	40	60	3
2	20ECC204	VLSI Design Verification and Testing	3	--	--	3	40	60	3
3		Program Elective-III	3	--	--	3	40	60	3
4		Program Elective-IV	3	--	--	3	40	60	3
5		Audit Course-II	2	--	--	2	--	50	Non-Credit
PRACTICALS									
6	20ECC207	RTL Simulation and Synthesis with PLDs Lab	--	--	4	--	50	--	2
7	20ECC208	RTOS and VLSI Design Verification Lab	--	--	4	--	50	--	2
8	20ECC209	Mini Project with Seminar	--	--	4	--	50	--	2
Total			**14**	**--**	**12**	**--**	**310**	**290**	**18**
Clock Hours Per Week: 26									

L: Lecture **D: Drawing** **CIE: Continuous Internal Evaluation**

T: Tutorial **P: Practical/Mini Project with Seminar/ Dissertation Phase** **SEE: Semester End Examination**

CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY (A)

(AICTE Model Curriculum with effect from AY 2020-21)

M.E (Embedded Systems & VLSI Design)

SEMESTER – III

S.No	Course Code	Title of the Course	Scheme of Instruction			Scheme of Examination			Credits
			Hours per week			Duration of SEE in Hours	Maximum Marks		
			L	T	P		CIE	SEE	
THEORY									
1		Program Elective-V	3	--	--	3	40	60	3
2		Open Elective	3	--	--	3	40	60	3
3	20ECC210	Dissertation Phase-I	--	--	20	--	100	--	10
Total			**6**	**--**	**20**	**--**	**180**	**120**	**16**
Clock Hours Per Week: 26									

L: Lecture **D: Drawing** **CIE: Continuous Internal Evaluation**

T: Tutorial **P: Practical/Mini Project with Seminar/ Dissertation Phase** **SEE: Semester End Examination**

CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY (A)

(AICTE Model Curriculum with effect from AY 2020-21)

M.E (Embedded Systems & VLSI Design)

SEMESTER – IV

S.No	Course Code	Title of the Course	Scheme of Instruction			Scheme of Examination			Credits
			Hours per week			Duration of SEE in Hours	Maximum Marks		
			L	T	P		CIE	SEE	
THEORY									
1	20ECC211	Dissertation Phase-II	--	--	32	Viva-Voce	100	100	16
Total			--	--	**32**	--	**100**	**100**	**16**
Clock Hours Per Week: 32									

L: Lecture **D: Drawing** **CIE: Continuous Internal Evaluation**

T: Tutorial **P: Practical/Mini Project with Seminar/ Dissertation Phase** **SEE: Semester End Examination**

List of Subjects for ME (ECE) Course with specialization in

EMBEDDED SYSTEMS & VLSI DESIGN

S.No	Course Code	Title of the Course
		Program Core Courses
1	20ECC201	Analog and Digital CMOS VLSI Design
2	20ECC202	Embedded System Design using RTOS
3	20ECC203	Microcontrollers and Programmable Digital Signal Processors
4	20ECC204	VLSI Design Verification and Testing
Practical Courses / Mini Project with Seminar/ Dissertation		
5	20ECC205	Analog and Digital CMOS VLSI Design Lab
6	20EC C206	Microcontrollers and Programmable Digital Signal Processors Lab
7	20ECC207	RTL Simulation and Synthesis with PLDs Lab
8	20ECC208	RTOS and VLSI Design Verification Lab
9	20ECC209	Mini Project with Seminar
10	20ECC210	Dissertation Phase-I
11	20ECC211	Dissertation Phase-II
Program Elective Courses		
1.	20EC E201	Advanced Computer Organization
2.	20EC E202	Communication Buses and Interfaces
3.	20EC E203	Data Acquisition System Design
4.	20EC E204	FPGA & CPLD Architectures
5.	20EC E205	Low Power VLSI Design
6.	20EC E206	Nano-materials and Nanotechnology
7.	20EC E207	Network Security and Cryptography
8.	20EC E109	Pattern Recognition and Machine Learning
9.	20EC E208	Programming Languages for Embedded Software
10.	20EC E209	RF IC Design
11.	20EC E210	SoC Design
12.	20EC E211	System Design with Embedded Linux
13.	20EC E212	VLSI Signal Processing
14.	20EC E213	VLSI Technology and Physical Design Automation
15.	20ECE114	Wireless Sensor Networks
Mandatory Course		
1	20ME C103	Research Methodology and IPR

S.No	Course Code	Audit Courses
1	20CE A101	Disaster Management
2	20EG A101	English for Research Paper Writing
3	20EG A102	Indian Constitution and Fundamental Rights
4	20IT A101	Pedagogy Studies
5	20EG A104	Personality Development through Life Enlightenment Skills.
6	20EE A101	Sanskrit for Technical Knowledge
7	20EG A103	Stress Management by Yoga
8	20EC A101	Value Education
Open Elective Courses		
1	20CS O101	Business Analytics
2	20ME O103	Composite Materials
3	20CE O101	Cost Management of Engineering Projects
4	20ME O101	Industrial Safety
5	20ME O102	Introduction to Optimization Techniques
6	20EE O101	Waste to Energy.

Note: Program Core /Program Elective of one specialization can be Program Elective for other specialization provided the condition for prerequisite is satisfied. However, a prior permission of the Chairman, BoS is to be obtained.

20ECC201

ANALOG AND DIGITAL CMOS VLSI DESIGN

Instruction	3L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Pre-requisites: Analog and Digital design concepts.

Course Objectives:
This course aims to:

1. Characteristic behavior of MOSFET, CMOSFET, FINFET, TFET, Meta Gate Technology.
2. Physical design concepts.
3. Design of Analog and digital circuits.

Course Outcomes:
Upon completion of this course, students will be able to:

1. Understand MOS structure, it's Behavior & fabrication process, various step in physical design flow of CMOS circuits, second order effects in MOS &ESD Models.
2. Design various types of combinational logic circuits and sequential logic circuits
3. Recall various advanced technologies in VLSI industry, the scaling issues, etc.
4. Analyze various analog amplifiers, Current mirror circuits and OP AMP
5. Design Basic Amplifiers, Current Mirrors, basic OPAMP, OP-AMP with different compensations.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	3	-	-	1	1
CO2	3	-	2	2	2
CO3	3	-	1	1	1
CO4	3	1	-	2	2
CO5	3	1	1	2	2

UNIT-I
Technology Scaling and Road map, Scaling issues, Standard 4 mask NMOS Fabrication process, Review: Basic MOS structure and its static behavior, Stick diagram and Layout, Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their evaluation of dynamic behavior, Power consumption.

UNIT-II
Physical Design Flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic ESD protection-human body model, Machine model, Combinational logic: Static CMOS design, Logic effort, Ratioed logic, Pass transistor logic, Dynamic logic Speed and power dissipation in dynamic logic Cascading dynamic gates, CMOS transmission gate logic.

UNIT-III

Sequential Logic: Static latches and registers, MUX based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, advanced technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology.

UNIT-IV

Introduction to Analog Design, Second order effects MOS small signal model, Single Stage Amplifier: Common Source Amplifier, CS Stage with Source Degeneration, Common Drain Amplifier & Common Gate Stage (resistive load) Current Mirrors: Basic Current Mirrors, Cascode Mirrors, Special Current Mirror, Single Stage Amplifier: Common Source Amplifier with Current source load, Triode load,CM Load, Frequency response of CS stage, Source follower, Common gate stage, Gilbert cell.

UNIT-V

MOS Difference Pair (One Stage OPAMP), Operational Amplifiers: Two stage OPAMP, Fully differential amplifiers, Slew rate, PSRR, Compensation of two- stage OPAMP, op-amp based comparator, switched capacitor. Introduction to data converters-specifications.

Text Books:

1. J P Rabaey, A P Chandrakasan, B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI series, 2nd edition 2003
2. David Johns, Ken Martin, "Analog Integrated Circuit Design", John Wiley & sons. 2004
3. Jacob Baker.R.et.al., "CMOS Circuit Design", IEEE Press, Prentice Hall, India, 2000

Suggested Reading:

1. Paul. R. Gray & Robert G. Major, "Analysis and Design of Analog Integrated Circuits", John Wiley & sons. 2004
2. Kang, S. and Leblebici, Y., "CMOS Digital Integrated Circuits, Analysis and Design", TMH, 3rdEdition 2003
3. BehzadRazavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill. 2002

20ECC202

EMBEDDED SYSTEM DESIGN USING RTOS

Instruction	3L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Prerequisites: The prior knowledge on the basics of operating systems.

Course Objectives:
This course aims to:

1. Understand the basic concepts of the UNIX operating system and POSIX Standards.
2. Know the importance of hard/soft Real-Time Systems and to familiarize the cases for tasks, semaphores, queues, pipes, and event flags.
3. Study the basics of the kernel objects and memory management in VxWorks and to know about real-time applications development tools.

Course Outcomes:
Upon completion of this course, students will be able to:

1. Understand the concepts of UNIX operating system and process management.
2. Describe the POSIX standards for real time systems and compare hard and soft real time systems.
3. Analyze various scheduling algorithms and application to real time systems.
4. Illustrate the concepts of real time operating system and VxWorks.
5. Elucidate the concepts software development tools and RTOS comparison.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	3	-	1	-	-
CO2	3	2	2	2	-
CO3	3	3	1	3	-
CO4	3	1	1	-	-
CO5	3	2	2	-	-

UNIT-I:
Brief Review of UNIX Operating Systems: UNIX Kernel File system concepts of Process Concurrent Execution &Interrupts. Process management – forks & execution. Programming with system calls, Process Scheduling, Shell programming and filters.Portable Operating system Interface (POSIX) IEEE Standard 1003.13 & POSIX real time profile. POSIX versus traditional Unix Signals. Overheads and timing predictability.

UNIT-II:
Hard versus Soft Real-time systems: Examples, Jobs & Processors, Hard and Soft timing constraints, Hard Real –time systems, SoftReal time systems. Classical Uniprocessor Scheduling algorithms –RMS, Preemptive EDF, Allowing for Preemptive and Exclusion condition.

UNIT-III:

Concept of Embedded operating systems, Differences between Traditional OS and RTOS, Real time system concepts, RTOS Kernel & Issues in Multitasking Task Assignment, Task switching, Foreground ISRs and Background Tasks, critical section, Reentrant Functions, Inter-process Communication (IPC)- IPC through Semaphores, Mutex, Mailboxes, Message queues or pipes and Event Flags.

UNIT-IV:

VxWorks –POSIX Real Time Extensions, timeout features, Task Creation, Semaphores (Binary, Counting), Mutex, Mailbox, Message Queues, Memory Management – Virtual to Physical Address Mapping.

UNIT-V:

Debugging tools and cross development environment, Software Logic analyzer, ICEs. Comparison of RTOS – VxWorks, µC/OS-II and RT Linux for Embedded Applications.

Text Books:

1. Jane W.S.Liu,"Real Time Systems", Pearson Education, Asia, 2001.
2. Wind River Systems, "VxWorks Programrs Guide", Wind River Systems Inc.2097.
3. Jean. J. Labrose, "MicroC/OS-II", The CMP Books, 2002**.**

Suggested Reading:

1. Betchof, D.R., "Programming with POSIX threads", Addison Wesley Longman, 2097.
2. C.M.Krishna and G.Shin, "Real Time Systems", McGraw-Hill Companies Inc., McGraw Hill International Editions, 2097

20ECC203

MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

Instruction	3L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Prerequisite: Microprocessor and its interfacing

Course Objectives:

This course aims to:

1. Learn about ARM Microcontroller architectural features
2. Understand the ARM'C' Programming for various applications
3. Study the DSP processor fundamentals and its development tools

Course outcomes:

Upon completion of this course, students will be able to:

1. Compare and select ARM processor core based on requirements of embedded application
2. Analyze various features of ARM Cortex-M Series Processor
3. Able to interface various I/OdevicestoARM7microcontrollers.
4. Understand the basic architectural needs of Programmable DSPs
5. Apply small applications on DSP processor-based platform

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	3	3	1	1	1
CO2	3	3	1	2	1
CO3	3	3	2	1	1
CO4	3	3	1	2	2
CO5	3	-	2	-	2

UNIT-I

Background of ARM and ARM Architecture :A Brief history, Architecture Versions, Registers, pipeline, exception, interrupts and the vector table; core extensions, Introduction to ARM instruction set, Introduction to Thumb instructions, Introduction to ARM C Programming.

UNIT-II

LPC21XX Microcontroller: Salient features of LPC 21XX, Pin description, Architectural Overview. Peripherals: Description of General- Purpose Input/ Output (GPIO)ports, Pin control Block. Features, Pin description, Register description and operation of PLL, Timers, PWM, Interfacing: LED, Relay, Buzzer, LCD, DAC, DC motor. Communication protocols: Brief overview on I2C, SPI and CAN.

UNIT-III

ARM Cortex-M3 Processor: The Thumb-2 Technology and Instruction Set Architecture, Programming model-Registers,Operation modes,Exceptions and Interrupts, Vector Tables, Memory Map, Applications.

UNIT-IV

Programmable DSP (P-DSP) Processors: Basic architectural features-VLIW architecture, DSP computational building blocks, Bus and Memory architecture, Address generation unit, speed issues, Fixed and Floating-point data paths, Introduction to TIDSP Processor family. Introduction to FPGA based DSP system design.

TMS320C67XX: Features of C67XX Processors, Internal Architecture, Functional units and operation, Data paths, Cross paths, Control Register File.

UNIT-V

TMS320C67XX Assembly Language Instructions: Functional Unit and its Instructions, Addressing modes, Fixed point Instructions, Conditional Operations, Parallel Operations, Floating point instructions.

TMS320C67XX Application Development Tools: Code composer studio (CCS), Application programs in C67XX Code development in both C and Assembly language.

Text Books:

1. JosephYiu,"ThedefinitiveguidetoARMCortex-M3",Elsevier,2nd Edition,2010
2. Andrew N. SLOSS, Domonic Symes, Chris Wright "ARM System Developers Guide-Designing and optimizing system software" ELSEVIER1st Edition2004.
3. Avatar Singh and S. Srinivasan, "Digital Signal Processing Implementations Using DSP Microprocessors", Thomson Brooks, 2004.

Suggested Reading:

1. B. Ventakaramani, M. Bhaskar, "Digital Signal Processes, Architecture Processing and Applications", Tata McGraw Hill, 2002.
2. RulphChassing, "Digital Signal Processing and Applications with the C6713 and C6416 DSK" A John Wiley & Sons, Inc., Publications.

20EC C204

VLSI DESIGN VERIFICATION AND TESTING

Instruction	3 L Hours per Week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Pre-requisite: Knowledge on Analog and Digital CMOS VLSI Design, C and C++ Language concepts.

Course Objectives:

This course aims to:

1. The concepts of verification and testing.
2. Data types and OOPs concepts.
3. Randomization in System Verilog.

Course Outcomes:

Upon completion of this course, students will be able to:

1. Recipe of front-end design verification techniques and create reusable test bench environments.
2. Understanding various data types used in System Verilog
3. Demonstrating OOPs concepts to System Verilog verification
4. Application of Randomization concept in System Verilog
5. Interface a System Verilog test bench with System C.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	3	3	2	1	1
CO2	3	2	1	2	1
CO3	3	2	1	1	1
CO4	3	0	1	2	1
CO5	3	2	1	2	2

UNIT-I

Verification Guidelines: Verification Process, Basic test bench functionality, directed testing, Methodology basics, Constrained-Random stimulus, Functional coverage, test bench components, Layered test bench, Building layered test bench, Simulation environment phases, Maximum code reuse, test bench performance.

UNIT-II

Data Types: Built-in data types, Fixed-size arrays, Dynamic arrays, Queues, Associative Arrays, Linked lists, Array methods, choosing a storage type, creating new types with typedef, Creating user-defined structures, Type conversion, Enumerated types, Constants strings, Expression width. Procedural statements and routines: Procedural statements, tasks, functions and void functions, Routine arguments, returning from a routine, local data storage, Time values.

UNIT-III

Basic OOPS: Introduction, think of nouns, not verbs, your first class, where to define a class, OOP terminology, creating new objects, Object de-allocation, using objects, Static variables vs. Global variables, Class methods, defining methods outside of the class, scoping rules, Using one class inside another.

UNIT-IV

Connecting the test bench and design: Separating the test bench and design, Interface constructs, Stimulus timing, Interface driving and sampling, connecting it all together, Top-level scope Program Module interactions. System Verilog Assertions, understanding dynamic objects, copying objects, Public vs. Local, straying off course building a test bench.

UNIT-V

Randomization: Introduction, What to randomize, Randomization in System Verilog, Constraint details solution probabilities, Controlling multiple constraint blocks, Valid constraints, In-line constraints, The pre randomize and post randomize functions, Random number functions, Constraints tips and techniques, Common randomization problems, Iterative and array constraints, Atomic stimulus generation vs. Scenario generation, Random control, Random number generators, Random device configuration.

Text Books:

1. Chris Spears, “System Verilog for Verification”, Springer, 2nd Edition 2006.
2. M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers 2002.

Suggested Reading:

1. Writing test benches using System Verilog By Janick Bergeron Edition: illustrated Published by Birkhäuser, 2006 ISBN 0387292217, 9780387292212
2. System Verilog for Verification: A Guide to Learning the Test bench Language Features by Chris Spear Edition: 2, Published by Springer, 2008 ISBN 0387765298, 9780387765297

20ECC205

ANALOG AND DIGITAL CMOS VLSI DESIGN LAB

Instruction	4P Hours per week
Duration of SEE	--
SEE	--
CIE	50 Marks
Credits	2

Pre-requisites: Analog and Digital design concepts.

Course Objectives:

This course aims to:

1. Understand Characteristics behavior of MOSFET.
2. Analyze performance of Differential amplifiers
3. Verify layout of basic digital circuits

Course Outcomes:

Upon completion of this course, students will be able to:

1. Verify the characteristics of MOSFET and design entry in the tool.
2. Understand and evaluate the design specs and library files of tool.
3. Apply the concept of theory and design in the lab implementation.
4. Analyze and calculation, power and delay from the graphs.
5. Compare performance of different circuits with the simulation results.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	3	3	3	3	3
CO2	3	3	3	3	3
CO3	3	3	3	3	3
CO4	3	3	3	3	3
CO5	3	3	3	3	3

List of Experiments:

1. Characteristics of MOSFET.
2. Calculation of rise time and fall time for CMOS inverter.
3. To build a three stage and five stage ring oscillator circuit in 0.18um and 0.13um technology and compare its frequencies and time period.
4. NMOS Common Source Amplifier.
5. Design of Differential Amplifier.
6. Design of Operational Amplifier.
7. Draw the layout of Inverter Circuit.

Suggested Reading:

1. Cadence Design Systems (Ireland) Ltd., “Cadence manual”, 2013.

20ECC206

MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS LAB

Instruction	4P Hours per week
Duration of SEE	--
SEE	--
CIE	50 Marks
Credits	2

Prerequisite: Programming in 'C' and basics of ARM Microcontroller.

Course Objectives:

This course aims to:

1. Write the ARM 'C' programming for applications
2. Understand the interfacing of various modules with ARM 7/ ARM Cortex-M3
3. Develop assembly and C Programming for DSP processors

Course Outcomes:

Upon completion of this course, students will be able to:

1. Install, configure and utilize tool sets for developing applications based on ARM processor core.
2. DesignanddeveloptheARM7 based embedded systems for various applications.
3. Develop application programs on ARM and DSP development boards both in assembly and C.
4. DesignandImplementthedigitalfiltersonDSP6713processor.
5. Analyze the hardware and software interaction and integration.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	2	1	3	1	1
CO2	2	1	3	1	1
CO3	2	1	3	1	1
CO4	2	1	3	1	1
CO5	2	1	3	1	3

List of Assignments:

Part A

ExperimentstobecarriedoutonARM7/Cortex-M 3 development boards

1. Blink an LED with software delay, delay generated using the Sys Tick timer.
2. System clock real-time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. UART EchoTest.

6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blink in grate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a micro-phone and display sound levels on LEDs.

Part B

Experiments to be carried out on DSP C6713 evaluation kits and using Code Composer Studio (CCS)

1. To develop assembly code and study the impact of parallel, serial and mixed execution
2. To develop assembly and C code for implementation of convolution operation
3. To design and implement IIR filters in assembly and in C to enhance the features of given input sequence/signal.
4. To design and implement FIR filters in assembly and in C to enhance the features of given input sequence/signal.

Suggested Reading:

1. Philipssemiconductors,"ARM7(LPC214x)usermanual",2005.
2. VinayK.Ingle and John G.Proakis, "Digital Signal Processing using MATLAB",4/e,Cengagelearning,2011.
3. B. Venkataramani and M. Bhaskar, "Digital Signal Processor architecture, programming and application",6/e,TMH,2006.
4. Rulph Chassing, "Digital Signal Processing and Applications with the C6713 and C6416 DSK" A John Wiley & Sons, Inc., Publications.

20ECC207

RTL SIMULATION AND SYNTHESIS WITH PLDs LAB

Instruction	4P Hours per week
Duration of SEE	--
SEE	--
CIE	50 Marks
Credits	2

Pre-requisites: Digital Design and Verilog HDL programming skills.

Course Objectives:

This course aims to:

1. The simulation of combinational and sequential circuits.
2. FSM based designs.
3. Implementation of DFT and FFTs.

Course Outcomes:

Upon completion of this course, students will be able to:

1. Demonstrate the process steps required for simulation /synthesis.
2. Design and simulate various combinational and sequential circuits using HDL.
3. Develop an RTL code for various real time applications.
4. Synthesize an RTL code for several digital designs.
5. Build a prototype for various digital circuits with PLDs.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	3	3	-	1	-
CO2	3	3	-	1	-
CO3	3	3	-	1	-
CO4	3	3	-	2	-
CO5	3	-	-	1	-

Design entry by Verilog, Programmable Logic Devices, Introduction to ASIC Design Flow, FPGA, SoC, Floor planning, Placement, Clock tree synthesis, Routing, Physical verification, Power analysis, ESD protection. Static Timing analysis, Meta-stability, Clock issues, Need and design strategies for multi-clock domain designs, IP and Prototyping, Design for testability.

List of Experiments:

1. Verilog implementation of 8:1 Mux/Demux, Full Adder, 8-bit Magnitude comparator,
2. Encoder/decoder, Priority encoder, D-FF, 4-bit Shift registers (SISO, SIPO, PISO, Bidirectional) 3-bit Synchronous Counters, Binary to Gray converter, Parity generator.
3. Sequence generator/detectors, Synchronous FSM – Mealy and Moore machines.
4. Vending machines - Traffic Light controller, ATM, elevator control.
5. PCI Bus & arbiter and downloading on FPGA.
6. UART/ USART implementation in Verilog.

7. Realization of single port SRAM in Verilog.
8. Verilog implementation of Arithmetic circuits like serial adder/subtractor, parallel adder/subtractor, serial/parallel multiplier.
9. Discrete Fourier transform/Fast Fourier Transform algorithm in Verilog.

Suggested Reading:

1. Samir Palnitkar, "Verilog HDL, a guide to digital design and synthesis", Prentice Hall 2003.
2. Doug Amos, Austin Lesea, Rene Richter, "FPGA based prototyping methodology manual", Xilinx, 2011.
3. Bob Zeidman, "Designing with FPGAs & CPLDs", CMP Books, 2002.

20ECC208

RTOS AND VLSI DESIGN VERIFICATION LAB

Instruction	4P Hours per week
Duration of SEE	--
SEE	--
CIE	50 Marks
Credits	2

Pre-requisites: Basics of operating system, basics of embedded system and verification concepts.

Course Objectives:

This course aims to:

1. Understand the concepts of RTOs
2. Illustrate the concept of task scheduling
3. Verify layout of basic digital circuits

Course Outcomes:

Upon completion of this course, students will be able to:

1. Verify a few important OOPs concepts
2. Compile and Run various design constructs using CAD tool
3. Develop self-checking test benches using SystemVerilog
4. Understand the programming concepts of RTOS
5. Analyze Multitasking, IPC and scheduling concepts

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	3	2	-	1	-
CO2	3	2	-	1	-
CO3	3	3	-	1	-
CO4	3	3	-	1	-
CO5	3	3	-	1	-

-

RTOS programming:

1. Introduction to RTOS (VxWorks) and its basic functions
2. RTOS Timer programming (VxWorks)
3. RTOS Task function programming (VxWorks)
4. Multitasking using round robin scheduling
5. IPC using message queues
6. IPC using semaphore
7. IPC using mail box

Verification (Mentor Graphics Tools)

1. Sparse memory
2. Semaphore
3. Mail box
4. Classes
5. Polymorphism
6. Coverage
7. Assertions

Suggested reading:

1. Silberschatz, Galvin, Gange"Operating Systems Concepts" 8/e , Wiley Education, 2007.
2. Wind River Systems Inc., "VxWorks Programmers Guide", 2097.

20EC C209

MINI PROJECT WITH SEMINAR

Instruction	4 P Hours per Week
Duration of SEE	--
SEE	--
CIE	50 Marks
Credits	2

Prerequisite: Knowledge of preparing slides by using power point presentations, Capable of searching for suitable literature and Presentation skills.

Course Objectives:

This course aims to:

1. The mini-project shall contain a clear statement of the research objectives, background of work, literature review, techniques used, prospective deliverables, and detailed discussion on results, conclusions and references.
2. To expose and practice of searching and referring the required literature.
3. This is expected to provide a good initiation for the student(s) towards R&D.

Course Outcomes:

Upon completion of this course, students will be able to:

1. Familiarize in searching the suitable literature in the chosen field.
2. Develop skills to understand and summarize the contents from the literature.
3. Ability to synthesize knowledge/ skills previously gained and applied in execution of a chosen technical problem.
4. Enhance oral presentation skills through power point presentations.
5. Learn and present the findings of their technical solution in a written report.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	1	-	3	3	3
CO2	1	-	3	3	3
CO3	2	-	3	3	3
CO4	2	-	3	3	3
CO5	2	-	3	3	3

Guidelines:

1. As part of the curriculum in the II - Semester of the Program each student shall do a mini project, generally comprising about three to four weeks of prior reading, twelve weeks of active research, and finally a presentation of their work for assessment.
2. Each student will be allotted to a faculty supervisor for mentoring.
3. Mini projects should present students with an accessible challenge on which to demonstrate competence in research techniques, plus the opportunity to contribute something more original.
4. Mini projects shall have inter-disciplinary/ industry relevance.

5. The students can select a mathematical modeling based/Experimental investigations or Numerical modeling.
6. All the investigations are clearly stated and documented with the reasons/explanations.
7. The mini project shall contain a clear statement of the research objectives, background of work, literature review, techniques used, prospective deliverables, and detailed discussion on results, conclusions and references.

Departmental committee: Supervisor and two faculty coordinators

Guidelines for awarding marks in CIE: Max. Marks: 50		
Evaluation by	**Max. Marks**	**Evaluation Criteria / Parameter**
Supervisor	20	Progress and Review
	05	Report
Departmental Committee	05	Relevance of the Topic
	05	PPT Preparation
	05	Presentation
	05	Question and Answers
	05	Report Preparation

20EC C210

DISSERTATION PHASE-I

Instruction	20 P Hours per Week
Duration of SEE	--
SEE	--
CIE	100 Marks
Credits	10

Prerequisite: Preferably, student must have completed 'Mini Project with Seminar' successfully.

Course Objectives:

This course aims to:

1. The Dissertation Phase-I (Project work) will preferably be a problem with research potential and should involve scientific research, design, generation/collection and analysis of data, determining solution and must preferably bring out the student contribution(s).
2. To expose and learn the required simulation software/experimental techniques.
3. To carry out the work in a research environment or in an industrial environment

Course Outcomes:

Upon completion of this course, students will be able to:

1. Survey the literature such as books, national/international refereed journals and contact resource persons for the selected topic of research/project field.
2. Consolidate the literature survey and will be motivated to define the title of the project, able to decide the aim(s), objectives and design specifications of the project.
3. Learn the required software/ computational/analytical tools for implementations.
4. Document a report comprising of summary of literature survey, detailed objectives, project specifications, or computer aided design, proof of concept/functionality, and part of results if any.
5. Get aquatinted to work in a research environment or in an industrial environment.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	1	2	3	3	3
CO2	2	2	3	3	3
CO3	2	2	2	3	3
CO4	2	2	2	3	3
CO5	2	2	2	3	3

Guidelines:

1. The Project work will preferably be a problem with research potential and should involve scientific research, design, generation/collection and analysis of data, determining solution and must preferably bring out the individual contribution.
2. Seminar should be based on the area in which the candidate has undertaken the dissertation work.
3. The CIE shall include reviews and the preparation of report consisting of a detailed problem statement and a literature review.
4. The preliminary results (if available) of the problem may also be discussed in the report.

5. The work has to be presented in front of the committee consists of Head, Chairperson-BoS, Supervisor and Project coordinator.
6. The candidate has to be in regular contact with his supervisor and the topic of dissertation must be mutually decided by the guide and student.

Guidelines for awarding Marks in CIE:		Max. Marks: 100
Evaluation by	**Max. Marks**	**Evaluation Criteria / Parameter**
Supervisor	40	Project Status / Review(s)
	20	Report
Departmental Review Committee	10	Relevance of the Topic
	10	PPT Preparation(s)
	10	Presentation(s)
	10	Question and Answers
	10	Report Preparation

Note: Departmental Review committee has to assess the progress of the student for every two weeks.

20EC C211

DISSERTATION PHASE-II

Instruction	32 P Hours per Week
Duration of SEE	Viva - Voce
SEE	100 Marks
CIE	100 Marks
Credits	16

Prerequisite: Student must have earned the credit of 'Dissertation Phase-I'.

Course Objectives:

This course aims to:

1. Dissertation Phase-II' is the continuation of Dissertation Phase-I'
2. Implementation of Project objectives.
3. Presentation of periodic reviews of the objectives and preparing of Dissertation in a prescribed format.

Course Outcomes:

Upon completion of this course, students will be able to:

1. Capable to select from different methodologies, methods and forms of analysis to produce a suitable research design, and justify their design.
2. Plan experiments for a critical comparison of outputs or to verify the obtained analytical/simulation results with the experimental results available in the literature.
3. Develop attitude of lifelong learning and will develop interpersonal skills to deal with people working in diversified field.
4. Learn to write technical reports and research papers to publish at national and international level.
5. Develop strong communication skills to defend their work in front of technically qualified audience.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	1	2	3	3	3
CO2	-	2	3	3	3
CO3	1	2	2	3	3
CO4	2	2	2	3	3
CO5	2	2	2	3	3

Guidelines:

1. It is a continuation of Project work started in semester III.
2. The student has to submit the report in prescribed format and also present a seminar.
3. The dissertation should be presented in standard format as provided by the department.
4. The candidate has to prepare a detailed project report consisting of introduction of the problem, problem statement, literature review, objectives of the work, methodology (experimental set up or numerical details as the case may be) of solution and results and discussion.
5. The report must bring out the conclusions of the work and future scope for the study. The work has to be presented in front of the examiners panel consisting of an approved external examiner, an internal examiner (HoD and BoS Chair Person) guide/co-guide.

6. The candidate has to be in regular contact with his/her guide/co-guide.

Guidelines for awarding marks in CIE:		Max. Marks: 100
Evaluation by	**Max. Marks**	**Evaluation Criteria / Parameter**
Departmental Review Committee	05	Review 1
	10	Review 2
	10	Review 3
	15	Final presentation with the draft copy of the report
	10	Submission of the report in a standard format
Supervisor	10	Regularity and Punctuality
	10	Work Progress
	10	Quality of the work which may lead to publications
	10	Analytical / Programming / Experimental Skills
	10	Report preparation in a standard format

Guidelines for awarding marks in SEE:		Max. Marks: 100
Evaluation by	**Max. Marks**	**Evaluation Criteria / Parameter**
External and Internal Examiner(s) together	20	Power Point Presentation
	40	Quality of thesis and evaluation
	20	Quality of the project • Innovations • Applications • Live Research Projects • Scope for future study • Application to society
	20	Viva-Voce

Note: Departmental Review committee has to assess the progress of the student for every two weeks.

20ECE201

ADVANCED COMPUTER ORGANIZATION

(Program Elective)

Instruction	3L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Prerequisite: Fundamentals of Computer architecture.

Course Objectives:

This course aims to:

1. Learn about processor design for computer system
2. Understand the memory organization of the computer
3. Study the I/O organization and parallel computer systems

Course Outcomes:

Upon completion of this course, students will be able to:

1. Analyze the computer arithmetic operations.
2. Design of control unit of the computer
3. Understand the memory organization of the computer
4. Interface various I/O modules to the computer system
5. Analyze the multiprocessor environment and various buses for the computer system.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	3	-	1	-	-
CO2	3	2	1	-	2
CO3	3	-	1	-	-
CO4	1	3	-	2	1
CO5	3	2	2	2	2

UNIT– I:

Processor Design: CPU Organization, Data Representation, Instruction Formats, Data Path Design: Fixed Point Arithmetic and Floating-Point Arithmetic, Instruction Pipelining, Super Scalar techniques, linear pipeline processors, Super scalar and super pipeline design, Multi vector and SIMD computers.

UNIT– II:

Control Unit Design:

Basic Concepts: Basic control unit of the computer system. Hardwired Control Unit Designapproach, Micro-programmed Control Unit- Design Approach, Micro program sequencer, Case studies based on both the approaches.

UNIT – III:

Memory Organization:

Internal memory, computer memory system overview, the memory Hierarchy, Random access memories, Cache memory, Elements of cache design, Virtual memory- protection and examples of virtual memory, Replacement Policies.

UNIT– IV:

I/O Organization: Accessing I/O Devices, Programmed I-O, Interrupts, DMA, Bus Arbitration; Synchronous bus and asynchronous bus, Interface circuits, Parallel port, Serial port, standard I/O interfaces, IO Processor, PCI bus, SCSI bus, USB busprotocols.

UNIT– V:

Parallel Computer Systems:

Instruction Level Parallelism (ILP) – Concept and Challenges, Dynamic Scheduling, Limitations on ILP, Thread Level Parallelism, Multi-processors – Characteristics, Symmetric and Distributive Shared Memory Architecture, Vector Processors and Supercomputers.

Text Books:

1. Carl Hamacher, Vranesic, Zaky, "Computer Organization", 5th edition, MGH, 2010
2. William Stallings, "Computer Organization and Architecture designing for Performance", 7th edition, PHI, 2007.

Suggested Reading:

1. John L. Hennessy and David A. Patterson, "Computer Architecture", A quantitative Approach, 3rd Edition, Elsevier, 2005.
2. Hayes John P, "Computer Architecture and organization" 3rd Edition, MGH, 2098.

20ECE202

COMMUNICATION BUSES AND INTERFACES

(Program Elective)

Instruction	3L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Prerequisite: Fundamentals of Computer organization and architecture.

Course Objectives:

This course aims to:

1. Learn about serial communication buses for computer system
2. Understand the CAN and PCI technology
3. Study the importance of the USB bus architecture

Course Outcomes:

Upon completion of this course, students will be able to:

1. Choose a particular serial bus suitable for a particular application.
2. Develop APIs for configuration, reading and writing data onto serial bus.
3. Design and develop peripherals that can be interfaced to desired serial bus.
4. Understand the CAN architecture and its applications
5. Analyze USB data transfers and descriptors and the PCI express technology.

UNIT-I

Serial Buses: Serial Port Advantages, Limits, Applications, System Components, Formats and Protocols Asynchronous and Synchronous Communications, Data Formats, Flow control.

UNIT-II

Serial COM Ports on PCs: RS232 -Signals, Voltages, Timing Limits, Interface chips; RS485 -Voltage requirements, Speed, Interfacing Options, Applications. SPI - Overview, Data and Control lines, Configuration; I^2C Overview, Protocol, Configuration.

UNIT-III

CAN: Architecture, Layered structure of a CAN node, Message Transfer - Arbitration, Frame types, Bit Stuffing, Applications.

UNIT-IV

PCI Express Technology (PCIe): PCI Express origins, Configuration space and Access Methods, Enumeration Process, Packet Types and Fields, Transaction Ordering, Traffic Classes, Virtual Channels and Arbitration (QoS), Flow Control, ACK/NAK Protocol, Applications.

UNIT-V

USB: Evolution, USB Vs Ethernet and IEEE-1394, bus components. USB Transfers: Types of Descriptors, Device endpoints, pipes, streams and message pipes. USB bus states, data encoding and Packet format. Introduction to Serial Front Panel Data Port (SFPDP).

Text Books:

1. Mike Jackson, Ravi Budruk, "PCI Express Technology", Mindshare Press, 1st edition, 2012
2. Jan Axelson, "Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems", Lakeview Research, 2nd Edition, 2012
3. Jan Axelson, "USB Complete", Penram Publications 3rd edition 2005.

Suggested Reading:

1. Wilfried Voss, "A Comprehensible Guide to Controller Area Network", Copperhill Media Corporation, 2nd Edition, 2005.

20ECE203

DATA ACQUISITION SYSTEM DESIGN

(Program Elective)

Instruction	3L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Pre-requisites: Concepts of Digital Systems and Communication Systems

Course Objectives:
This course aims to:

1. Understand the different types of communication interface buses.
2. Familiarize different methods of ADC's and DAC's characteristics, specifications
3. Study the software tools to develop the code and implementation for data acquisition system

Course Outcomes:
Upon completion of this course, students will be able to:

1. Understand the fundamentals of sensors, transducers and signal conditioning.
2. Explain configuration of computer plugin I/O standalone and distributed loggers controllers.
3. Demonstrate the Interface of the hardware for acquiring the data through systems.
4. Build the design flow for data acquisition system.
5. Experiment with software tools to develop the code and implementation for data acquisition system.

UNIT-I:
Fundamentals of Data Acquisition Systems,Sensors and Transducers,Signal conditioning - Introduction, Types of signal conditioning, Classes of signal conditioning, DAQ Hardware, DAQ Software, Communications Cabling, Parameters of a DAQ System.

UNIT-II:
Data acquisition system configuration, Computer plug in I/O, Distributed I/O, Stand-alone or distributed loggers/controllers- Introduction, Methods of operation, Stand-alone logger/controller hardware, firmware & software design, Communications hardware interface, Host software, Considerations, internal systems, USB overall structure, PCMCIA card.

UNIT-III:
Data Acquisition Systems: Hardware-Introduction, Plug-in DAQ Systems, Converters A/D, Converters D/A, Amplifier, Multiplexer/De-multiplexer, Power Management, Timing System, Filtering, Memory Board, Bus Interface.

UNIT-IV:

Communication Bus-Bus and FireWire, Serial Communications, Wireless, Ethernet and Bluetooth,GSM for Data Acquisition System, PCI and PCI Express, Standard VME.

UNIT-V:

D**esign of Data Acquisition System**: Introduction to the Design, Functional Design of high-Speed Computers-Based DAS, Portable DAS, Design Guidelines for High-Performance Multichannel.Software for Data Acquisition Systems, Introduction to LabVIEW, Android for DAQ, Design of Firmware, Example of Implementation of a Software.

Text Books:

1. Maurizio Di Paolo Emilio "Data acquisition systems-from fundamentals to applied design" springer, 2013.
2. John Park and Steve Mackay "Practical Data acquisition for instrumentation and control systems" Elsevier, 2003.

Suggested Reading:

1. Robert H King, "Introduction to Data Acquisition with LabVIEW", 2nd edition, 2012, McGraw Hill.

20ECE204

FPGA AND CPLD ARCHITECTURES

(Program Elective)

Instruction	3L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Pre-requisites: Knowledge of Digital design using Multiplexers and Look-up tables.

Course Objectives:
This course aims to:

1. Study various PLD, CPLDs and FPGA Architectures and its features.
2. Understand the different programming technologies, placement and routing.
3. Study the design tools for FPGA and ASICs.

Course Outcomes:
Upon completion of this course, students will be able to:

1. Explain the concepts of PLDs, CPLDs and FPGAs.
2. Analyze and compare the various architectures of CPLD and FPGA and its programming technologies.
3. Implement various logic functions on PLDs, CPLDs and FPGAs.
4. Understand the concepts of placement and routing algorithms and classifying ASICs.
5. Demonstrate VLSI tool flow for CPLDs and FPGAs.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	3	-	-	-	1
CO2	3	2	-	1	-
CO3	2	3	1	2	2
CO4	3	3	3	2	2
CO5	3	3	3	2	2

UNIT-I:

Programmable Logic Devices: Introduction, Evolution: Programmable read only memory (PROM), programmable logic array (PLA) and programmable array logic (PAL). Implementation with PLDs, Programming technologies. Design flow for CPLDs & FPGAs.

UNIT-II:

CPLDs: Complex Programmable Logic Devices: Architecture and features of Altera max 6000 series CPLD, AMD Mach 4 and Xilinx 9500 series.

FPGAs: Field Programmable Gate Arrays: Logic blocks, routing architecture and features of Xilinx XC4000, Spartan II, Virtex II and Actel Act1, Act2, Act3 FPGAs.

UNIT-III:

Advance FPGAs: Architectures and Features of Xilinx Spartan- 6, Virtex-6, and AlterasStartix FPGAs. Introduction to Xilinx Zynq board.

UNIT-IV:

Placement: objectives, placement algorithms: Min-cut-Based placement, Iterative Improvement placement, Simulated Annealing. Routing: objectives, Segmented Channel Routing, Maze Routing, Routability estimation, computing signal delay in RC tree networks.

UNIT-V:

Digital Front End and backEnd tools for FPGAs and ASICs, FPGA implementation steps. Verification: introduction, logic simulation, design validation, timing verification. Testing concepts: failures, mechanisms and faults, fault coverage, ATPG methods and programmability failures.

Text Books:

1. S. Brown, R. Francis, J. Rose, Z.Vransic, “Field Programmable Gate array”, BSP,2007.
2. P.K. Chan & S. Mourad, “Digital Design Using Field Programmable Gate Array”, Pearson Education 2009.

Suggested Reading:

1. S. Trimberger, Edr., “Field Programmable Gate Array Technology”, Kluwer Academic Publications, 2094**.**

20EC E205

LOW POWER VLSI DESIGN

(Program Elective)

Instruction	3L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Pre-requisites: Students should have prior knowledge of Analog and Digital CMOS VLSI Design.

Course Objectives:

This course aims to:

1. Know the sources of power dissipation and need for low power designs for emerging technologies.
2. Understand the concepts of Low power design techniques for digital circuits.
3. Analyze the power dissipations of memory and processor systems and able to adopt suitable methods for power reduction.

Course Outcomes:

Upon completion of this course, students will be able to:

1. Identify sources of power dissipation in a given VLSI Circuit
2. Analyze and apply various low power circuit techniques for combinational and sequential circuits
3. Demonstrate understanding of clock distribution for Low Power
4. Elaborate Microprocessor Design System concepts for Low Power
5. Explain power estimation techniques for memory subsystem.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	3	-	2	2	-
CO2	3	2	-	2	-
CO3	3	3	-	2	-
CO4	3	-	-	-	-
CO5	3	3	2	1	-

UNIT-I:

Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of V_{dd}&V_t on speed, constraints on Vt reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations.

UNIT-II:

Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

UNIT-III:

Low Power Clock Distribution: Power dissipation in clock distribution, single driver Versus distributed buffers, buffers & device sizing under process variations, zero skew vs Tolerable skew, chip & package co-design of clock network.

UNIT-IV:

Logic Synthesis for Low Power estimation techniques: Power minimization techniques, Low power arithmetic components-circuit design styles, adders, multipliers. Low Power Memory Design: Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM.

UNIT-V:

Low Power Microprocessor Design System: power management support, architectural tradeoffs for power, choosing the supply voltage, low-power clocking, implementation problem for low power, comparison of microprocessors for power & performance.

Text Books:

1. Jan M. Rabaey and MassoudPedram, "Low Power Design Methodologies", Kluwer Academic, 2096
2. Kaushik Roy, Sharat Prasad, "Low power CMOS VLSI circuit design", John Wiley sons, Inc., 2000.

Suggested Reading:

1. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley, 2099.
2. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 2098.
3. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer,2095

20EC E206

NANO-MATERIALS AND NANOTECHNOLOGY

(Program Elective)

Instruction	3 L Hours per Week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Prerequisite: Basic knowledge in Nano Materials and Material Science.

Course Objectives:

This course aims to:

1. Describe the basic science behind the properties of materials at the Nanometer scale.
2. Understand the various micro and nano fabrication techniques
3. Characterize Nano Structures and special Nano Materials.

Course Outcomes:

Upon completion of this course, students will be able to:

1. Understand the basic electrical and optical, magnetic, mechanical properties of nano materials.
2. Construct devices based on nano materials.
3. Explain nano fabrication steps, fabrication and applications of MEMS.
4. Construct Nano structures like Carbon nano tubes and MEM actuators.
5. Discuss various procedures of nano composites and applications of nano biomaterials.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	1	1	1	1	1
CO2	2	1	1	1	1
CO3	2	2	2	2	2
CO4	2	2	3	2	3
CO5	3	3	3	2	3

UNIT-I

Introduction to Nano Materials: Evolution of Nano-science and technology, Introduction to Nanotechnology, Moore's law, Bottom up and Top – down approaches, Introduction to Semiconducting Nano particles, Electrical and optical properties, Superconducting properties, magnetic properties, mechanical properties.

UNIT-II

Applications of Nano-materials: Molecular Electronics and Nano-electronics, Nanobots,Biological Applications of Nanoparticles, Catalysis by Gold Nano-particles, Band Gap Engineered Quantum Devices-

Quantum well devices, Quantum dot devices, Nano-mechanics, Carbon Nanotube Emitters. Photo-electro-chemical Cells, Photonic Crystals and Plasmon Waveguides.

UNIT-III

Nano Fabrication: Introduction to Micro, Nano fabrication, Lithography, Electron beam lithography, thin film deposition. Nano and Micro-electromechanical systems (NMEMS), Types of MEMS, Fabrication of MEMSassembling and packaging, applications of MEMS.

UNIT-IV

Nano Structures: Carbon Nanotubes and Nano devices-structural design of Nano and MEM actuators and sensors configurations and structural design of motion Nano and micro- structures.

UNIT-V

Special Nano Materials: Nano Composites- Introduction, Synthesis procedures, various systems (metal polymer and metal ceramics) characterization procedures, applications.
Nano Biomaterials: Introduction, Biocompatibility, applications.

Text Books:

1. Guozhongcao, “Nano Structures and Nano materials: Synthesis, properties and applications”, Imperial college press, 2004.
2. Lyschevski, Sergey Edward, “Nano and Microelectro Mechanical Systems”, Fundamentals of Nano and micro engineering, CRC Press, 2000.

Suggested Reading:

1. A S Edelstein & R C Cammarata, “Nano Materials: Synthesis, Properties, and Applications”, Institute of physics publishing, 2096.

20ECE207

NETWORK SECURITY AND CRYPTOGRAPHY

(Program Elective)

Instruction	3 L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Prerequisite: Concepts of Data Computer and Communication Networks.

Course Objectives:

This course aims to:

1. Understand the concepts of public key and private key cryptography techniques
2. Study about message authentication and digital signatur standards
3. Impart the knowledge of system security

Course Outcomes:

Upon completion of this course, students will be able to:

1. Identify and utilize different forms of cryptography techniques.
2. Analyze solutions for effective key management and distribution and conduct crypt analysis
3. Predict Encryption and decryption of data using Symmetric key and Asymmetric ciphers
4. Assess authentication and security in the network applications.
5. Interpret different types of threats to the system and handle the same.

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CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	1	1	2	2	1
CO2	2	1	1	1	2
CO3	3	2	1	3	2
CO4	3	3	3	2	2
CO5	3	3	3	3	3

UNIT-I

Security: Need, security services, Attacks, OSI Security Architecture, one-time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques

UNIT-II

Private-Key (Symmetric) Cryptography : Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard(DES),Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

UNIT-III

Public-Key (Asymmetric) Cryptography: RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4, MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

UNIT-IV

Authentication: IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer and Transport Layer Security, Secure Electronic Transaction.

UNIT-V

System Security: Intruders, Intrusion Detection, Password Management, Worms, Viruses, Trojans, Virus Countermeasures, Firewalls, Firewall Design Principles, Trusted Systems.

Text Books:

1. William Stallings, "Cryptography and Network Security, Principles andPractices",Pearson Education,6th Edition,2013.
2. Charlie Kaufman, Radia Perlman and Mike Speciner,"Network Security, Private Communicationina Public World", Prentice Hall, 2nd Edition,2095.

Suggested Reading:

1. Stephen Northcutt, LenyZeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "Inside Network Perimeter Security", Pearson Education,2nd Edition,2005.
2. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident detection and Response", William Pollock Publisher,2013.

20ECE109

PATTERN RECOGNITION AND MACHINE LEARNING

(Program Elective)

Instruction	3L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Pre-requisites: The student should have knowledge of probability and random variables.

Course Objectives:
This course aims to:

1. Understand, design and evaluate pattern recognition problems.
2. Design and implement machine learning solutions to classification
3. Evaluate and interpret the results of the algorithms.

Course Outcomes:
Upon completion of this course, students will be able to:

1. Understand the concepts of pattern recognition.
2. Apply the parametric and linear models for classification.
3. Design algorithms using neural networks for machine learning problems.
4. Implementation of Support Vector Machines (SVM) algorithm for real time applications.
5. Evaluate various unsupervised clustering techniques.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	2	1	2	2	1
CO2	1	1	1	1	2
CO3	3	2	2	3	2
CO4	2	2	3	1	3
CO5	3	3	3	3	3

UNIT-I

Introduction to Pattern Recognition: Pattern Recognition Systems, applications, design cycle, learning and adaptation, examples, Probability Distributions, Bayesian Decision Theory-continuous Features, Minimum Error rate classification, Classifiers, Discriminant Functions and Decision surfaces, Bayesian Decision Theory- Discrete Features. Maximum-Likelihood and Bayesian parameter estimation: Maximum Likelihood estimation, Bayesian estimation.

UNIT-II

Linear Models: Linear Models for Regression: Linear Basis Function Models, The Bias -Variance

Decomposition, Bayesian Linear Regression, Linear Models for Classification: Discriminant Functions, Probabilistic Generative Models, Probabilistic Discriminative Models, Bayesian Logistic Regression.

UNIT-III

Neural Network: Feed forward operation and classification: Multilayer Networks, back propagation algorithm: Network learning, training protocols, Learning Curves, error surfaces, practical techniques for improving back propagation, additional networks and training methods, Adaboost, Deep Learning.

UNIT-IV

Linear Discriminant Functions: Decision surfaces: Two category case and multi category case, two-category Linearly separable case, Minimum- squared error procedures, the Ho-Kashyap procedures, linear programming algorithms, Support vector machines.

UNIT-V

Algorithm Independent Machine Learning: lack of inherent superiority of any classifier, bias and variance, re-sampling for classifier design, combining classifiers.

Unsupervised Learning and Clustering: k-means clustering, fuzzy k-means clustering, Hierarchical clustering.

Text Books:

1. C.Bishop, "Pattern Recognition and Machine Learning", Springer, 2006.
2. Richard O.Duda, Peter E.Hart and David G.Stork, "Pattern Classification", 2nd Edition John Wiley & Sons, 2001.

Suggested Reading:

1. B.Yagnanarayana, Artificial Neural Networks, Prentice Hall, New Delhi, 2007.

20EC E208

PROGRAMMING LANGUAGES FOR EMBEDDED SOFTWARE

(Program Elective)

Instruction	3L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Pre-requisites: Embedded systems and C programming.

Course Objectives:

This course aims to:

1. Introduce students to various programming languages like C, C++,Java script, PERL, etc.
2. Distinguish between Procedural and OOP language, Introduce features of OOPs etc.
3. Demonstrate the development of some typical applications using different Programming languages.

Course Outcomes:

Upon completion of this course, students will be able to:

1. Develop embedded C application of moderate complexity.
2. Build the Object-Oriented approach to software that models application and Develop algorithms inC++.
3. Understand the overloading and Inheritance concepts of programming.
4. Assess the exceptions of the error code.
5. Differentiate interpreted languages from compiled languages.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	3	1	2	2	1
CO2	2	1	1	2	1
CO3	2	1	1	2	1
CO4	1	1	1	2	1
CO5	2	1	2	2	1

UNIT-I:

Embedded 'C' Programming: Bitwise operations, Dynamic memory allocation, OS services, linked stack and queue, Sparse matrices, Binary tree, Interrupt handling in C, Code optimization issues, Writing LCD drives, LED drivers, Drivers for serial port communication, Embedded Software Development Cycle and Methods (Waterfall, Agile).

UNIT-II:

Object Oriented Programming: Introduction to procedural, modular, object oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data Abstraction and information hiding, inheritance, polymorphism.

UNIT-III:

CPP Programming: 'cin', 'cout', formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, 'this' pointer, constructors, destructors, friend function, dynamic memory allocation.

UNIT-IV:

Overloading and Inheritance: Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance.

Templates: Function template and class template, member function templates and template arguments.

UNIT-V:

Exception Handling: Syntax for exception handling code: try-catch-throw, Multiple Exceptions.

Scripting Languages: Overview of Scripting Languages – PERL, CGI, VB Script, Java Script.

PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation & Line Interfacing.

Text Books:

1. Michael J. Pont , "Embedded C", Pearson Education, 2ndEdition,2008
2. Robert Sedgewick, "Algorithms in C++", Addison Wesley PublishingCompany, 2099.

Suggested Reading:

1. Randal L. Schwartz, "Learning Perl", O'Reilly Publications, 6th Edition2011
2. Michael Berman, "Data structures via C++", Oxford UniversityPress, 2002

20ECE209

RF IC DESIGN

(Program Elective)

Instruction	3L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Prerequisite: Network Theory, Analog Electronics, CMOS VLSI.

Course Objectives:

This course aims to:

1. Introduce students the concept of tuned circuit, matching network, reflection coefficients, transmission lines and MOS high frequency behavior etc.
2. Demonstrate design of High Frequency Amplifiers.
3. Introduce various types of Power Amplifiers and PLLs

Course Outcomes:

Upon completion of this course, students will be able to:

1. Define and understand the characteristics RF systems, Tuned circuits, LNA, Mixers.
2. Understand the behavior of RF systems, Reflection Coefficient and Noise in the MOS device.
3. Apply the concepts noise and to characterize the amplifiers.
4. Analyze different Power Amplifiers at RF range; design different LNA Configuration, Power Amplifiers.
5. Design and Develop a PLL for the given specifications.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	3	-	1	-	-
CO2	3	-	-	2	2
CO3	3	-	1	2	2
CO4	3	-	1	2	2
CO5	3	-	1	2	2

UNIT-I

RF Tuned Circuits: RF systems – Basic architectures, Maximum Power Transfer, Passive RLC Networks, Parallel RLC tank, Q, Series RLC networks, matching, Pi match, T match, Passive components in IC: Resistors, capacitors, Inductors, Transceiver Architectures.

UNIT-II

Nonlinearity and Reflection Coefficient: Nonlinearity and Time Variance of system, sensitivity and dynamic range, Review of MOS Device Physics, MOS device review, Distributed Systems, Transmission lines, reflection coefficient, the wave equation Lossy transmission lines Smith charts – plotting gamma, Noise in FET: Thermal noise, flicker noise review.

UNIT-III

High Frequency Amplifier Design: Bandwidth estimation using open-circuit time constants, Bandwidth estimation using short-circuit time constants, Rise-time, delay and bandwidth, Zeros to enhance bandwidth, Shunt-series amplifiers, tuned amplifiers Cascaded amplifiers, Noise figure, Intrinsic MOS noise parameters, LNA Design, Power match versus noise match.

UNIT-IV

RF Power Amplifiers: Multiplier based mixers, Subsampling mixers & Mixer Design, RF Power Large signal performance Amplifiers, Class A, AB, B, C amplifiers, Class D, E, F amplifiers, RF Power amplifier design issues.

UNIT-V

PLL: Voltage controlled oscillators, Resonators, Negative resistance oscillators, Phase locked loops, Linearized PLL models, Phase detectors, charge pumps, Loop filters, PLL design examples, Frequency synthesis and oscillator Frequency division, integer-N synthesis, Fractional frequency synthesis, Phase noise.

Text Books:

1. Thomas H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits", Cambridge University Press, 2004.
2. Behzad Razavi, "RF Microelectronics", Prentice Hall, 2097**.**

Suggested Reading:

1. Abidi, P.R. Gray, and R.G. Meyer, eds., "Integrated Circuits for Wireless Communications", New York: IEEE Press, 2099.
2. R. Ludwig and P. Bretchko, "RF Circuit Design, Theory andApplications", Pearson, 2000

20EC E210

SOC DESIGN

(Program Elective)

Instruction	3L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Pre-requisites: Concept of Embedded Systems, Microprocessors, microcontrollers and ASIC.

Course Objectives:

This course aims to:

1. Introduce students to various approaches of SoC design, ADLs and GNR.
2. Introduce various techniques used for Low power SoC Design
3. Demonstrate various simulation methods and synthesis techniques for SoCs.

Course Outcomes:

Upon completion of this course, students will be able to:

1. Understand the conceptsrelated to SoC like NISC, ASIP, ADL, GNR, Reconfiguration, Clock Gating, DVS etc.
2. Differentiate between various design strategies like ASIC and SOC etc.
3. Distinguish between various types of Processors like CISC, RISC, NISC and ASIP.HDL and ADL
4. Design a simple SOC for reconfigurability / low power / ASIP / NISC etc. and synthesize simple blocks using Graph Theory.
5. Simulate and synthesize the Design using various simulation models.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	3	3	1	3	2
CO2	3	3	2	3	2
CO3	3	1	1	3	2
CO4	3	3	2	3	2
CO5	3	-	1	-	-

UNIT 1

ASIC and NISC Overview: Overview-Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts, NISC-NISC Control Words methodology, NISC Applications and Advantages.

UNIT 2

ADL (for ASIP&NISC) and GNR: Architecture Description Languages (ADL) for design and verification of Application Specific Instruction-set Processors (ASIP), NISC-design flow, modeling NISC architectures and systems,

Generic Netlist Representation -A formal language for specification, compilation and synthesis of embedded processors.

UNIT 3

Low power SoC design: Low power SoC design / Digital system, Low power system perspective-power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, power down techniques, power consumption verification.

UNIT 4

Simulation: Different simulation modes, behavioral, functional, static timing, gate level,switch level, transistor/circuit simulation, design of verification vectors.FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

UNIT 5

Synthesis: Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis. HDL coding techniques for minimization of power consumption.Designof NISC for DCT application.

Text Books:

1. Michael J. Flynn and Wayne Luk, “Computer System Design: Systemon-Chip”. Wiley, 2011.
2. B. Al Hashimi, “System on chip-Next generation electronics”, The IET, 2006.

Suggested Reading:

1. Hubert Kaeslin, “Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication”, CambridgeUniversity Press, 2008.
2. RochitRajsuman, “System-on- a-chip: Design and test”, Advantest America R & D Center, 2000.
3. P Mishra and N Dutt, “Processor Description Languages”, Morgan Kaufmann, 2008

20EC E211

SYSTEM DESIGN WITH EMBEDDED LINUX

(Program Elective)

Instruction	3L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Pre -requisite: Fundamentals of Computer organization and architecture, Embedded Systems.

Course Objectives:

This course aims to:

1. Introduce student to the need of Embedded Linux and to Differentiate between Desktop and Embedded Linux.
2. Introduce students to different Board support packages and Divers for Embedded Linux
3. Demonstrate Embedded Linux development cycle and use of Memory Management.

Course Outcomes:

Upon completion of this course, students will be able to:

1. Understand the importance of Embedded Linux in system design.
2. Analyze the architecture of Embedded Linux in detail.
3. Explain the Linux BSP for a hardware platform.
4. Develop and Debug the drivers in Embedded Linux.
5. Apply the concepts of μClinuxto System design.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	1	1	1	3	1
CO2	2	1	2	3	1
CO3	3	1	2	2	1
CO4	3	2	2	2	1
CO5	2	2	2	3	1

UNIT-I

Introduction: Need of Embedded Linux, Embedded Linux versus Desktop Linux, Embedded Linux Distributions

Embedded Linux Architecture, Kernel Architecture: Hardware Abstraction Layer (HAL), Memory Manager, Scheduler, File System, IO Subsystem, Networking Subsystems, IPC; User Space, Linux Start-Up Sequence.

UNIT-II

Board Support Package: Inserting BSP in Kernel Build Procedure, the Boot Loader Interface, Memory Map, Interrupt Management, the PCI Subsystem, Timers, UART, and Power Management. Embedded Storage: Flash Map, Memory Technology Device, MTD Architecture, Embedded File Systems.

UNIT-III

Embedded Drivers: Linux Serial Driver, Ethernet Driver, and I2C Subsystem on Linux, USB Gadgets, Watchdog Timer, and Kernel Modules. Porting Applications: Architectural Comparison, Application Porting Roadmap.

UNIT-IV:

Real-Time Linux: Linux and Real-Time;Building and Debugging: Building the Kernel, Building the Root File System, Integrated Development Environment, Elementary Concepts of Debugging. Embedded Graphics: Graphics System, Introduction to Display Hardware.

UNIT-V:

uClinux: Linux on MMU - Less Systems, Program Load and Execution, Memory Management, File / Memory Mapping.

Text Books:

1. Derek Molloy, "Exploring Beagle Bone: Tools and Techniques for Building with Embedded Linux", Wiley, 1st Edition, 2014.
2. Christopher Hallinan, "Embedded Linux Primer: A Practical Real-World Approach", Prentice Hall, 2nd Edition, 2010.

Suggested Reading:

1. P Raghvan, Amol Lad, SriramNeelakandan, "EmbeddedLinux System Design and Development", Auerbach Publications, 2005.
2. KarimYaghmour, "Building Linux Systems", O'Reilly & Associates,2008.

20ECE212

VLSI SIGNAL PROCESSING

(Program Elective)

Instruction	3L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Pre-requisites: VLSI Design, signals and systems and DSP concepts.

Course Objectives:

This course aims to:

1. Understand fundamentals of DSP systems
2. Impart the knowledge of Pipelined and parallel recursive and adaptive filters
3. Analyze the Systolic architecture design concepts

Course Outcomes:

Upon completion of this course, students will be able to:

1. Understand the concepts of various DSP algorithms, its DFG representation, pipelining and parallel processing approaches
2. Demonstrate retiming techniques and systolic architecture design concepts
3. Develop various convolution algorithms for programmable hardware.
4. Evaluate pipelining and parallel processing techniques in the design of recursive digital filters
5. Discuss algorithmic strength reduction techniques and evolution of DSP processors.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	1	1	1	3	1
CO2	2	1	2	3	1
CO3	3	1	2	2	1
CO4	3	2	2	2	1
CO5	2	2	2	3	1

UNIT-I:

Introduction to DSP systems, Typical DSP algorithms, DSP Application Demands and scaled CMOS technologies**:** Iteration Bound- Data Flow Graph representations, Loop bound and Iteration bound, algorithm for computing iteration bound, iteration bound of multi-rate Data Flow Graph.

UNIT-II:

Retiming - Definitions and properties, solving systems of inequalities, Retiming techniques, Unfolding-Algorithm, properties, critical path, application. Algorithmic strength reduction in filters andTransforms-Parallel FIR filters, DCT and inverse DCT, Parallel architectures for rank order filters.

UNIT-III:

Systolic architecture design: Systolic array design methodology, FIR Systolic Arrays, Selection of scheduling vector, Matrix –Matrix Multiplication and 2D- Systolic Array design, Systolic design for space Representations containing delays.Fastconvolution: Cook-Toom Algorithm, Winograd-Algorithm, Iterated convolution, cyclic convolution, design of fast convolution algorithm by inspection.

UNIT-IV:

Pipelined and parallel recursive andadaptive filters: Pipeline interleaving, parallel processing and combined, Scaling and round off noise- computation.Digital lattice filter structures, Bit level arithmetic, architecture, redundant arithmetic.

UNIT-V:

Numerical strength reduction, synchronous, wave and asynchronous pipelines, Programmable digit signal processors.

Text Books:

1. Keshab K. Parthi, "VLSI Digital signal processing systems, design and implementation", Wiley, Inter Science, 2099.
2. Mohammad Isamail and Terri Fiez, "Analog VLSI signal and information processing", McGraw Hill, 2094.
3. S.Y. Kung, H.J. White House, T. Kailath, "VLSI and Modern Signal Processing", Prentice, Hall, 2085.

Suggested Reading:

1. U. Meyer -Baese, Digital Signal Processing with FPGAs, Springer, 2004.

20ECE213

VLSI TECHNOLOGY AND PHYSICAL DESIGN AUTOMATION

(Program Elective)

Instruction	3 L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Prerequisite: Basic knowledge on semiconductor physics and MOS transistors followed by analog and digital
Fundamentals is required.

Course Objectives:
This course aims to:

1. Model passive and active devices suiting advances in IC fabrication technology.
2. Create learning, development and testing environment to meet ever challenging needs in the field of Chip Design.
3. Communicate effectively and convey ideas using innovative engineering using appropriate EDA tools

Course outcomes:
Upon completion of this course, students will be able to:

1. Explain various technology aspects of VLSI Physical design.
2. Demonstrate CMOS IC fabrication process.
3. Apply Design rules in the construction of layouts of a given design.
4. Choose appropriate Automation algorithm for partitioning, floor planning, placement and routing.
5. Identify EDA/CAD tools for Automation of VLSI Physical design automation.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	3	1	3	3	1
CO2	3	1	3	3	1
CO3	3	1	3	3	2
CO4	3	1	2	3	1
CO5	3	1	2	3	2

UNIT-I

Introduction to VLSI Technology and Fabrication Process: Various layers of IC, Wafer preparation and crystal growth, Oxidation, CVD, Lithography, Etching, Ion implantation, Diffusion techniques.

UNIT-II

Concepts and Scope of Physical Design: Typical structures of passive and active components, CMOS fabrication process- n-Well, P-Well and Twin Tub, CMOS parasitic- Latch-up and its prevention.

UNIT-III

Cell Concepts and Design Rules: Cell based layout design, fabrication errors, alignment sequence and alignment inaccuracy, Interconnects, Contacts, Vias, SCMOS design rules, Lambda based design rules, Stick diagrams, Hierarchical stick diagrams, Layouts.

UNIT-IV

General Purpose Methods for Combinational Optimization: Partitioning, Placement, Discrete methods of global and local placements, Routing, local and Global routing via minimization, Over the cell routing, Single layer and two-layer routing, Clock and power routing.

UNIT-V

EDA/CAD Tools: Layout editors, Circuit extractors, Automatic layout tools, Modeling and extraction of circuit Parameters from physical layout, Compaction algorithms, physical automations of FPGAs.

Text Books:

1. J.D.Plummer, M.D.Deal and P.B.Griffin, "The Silicon VLSI Technology Fundamentals", Practice and modeling, Pearson Education 2009.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", 2002.

Suggested Reading:

1. Modern VLSI Design (System on Chip), Woyne Wolf, Pearson Education, 2002.
2. S.H. Gerez, "Algorithms for VLSI Design Automation", 2098.

20ECE114

WIRELESS SENSOR NETWORKS

(Program Elective)

Instruction	3 L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Pre-requisites: The knowledge of Wireless/Mobile communications is essential.

Course Objectives:

This course aims to:

1. Understanding of Sensor node architecture with hardware and software details for data storage and data dissemination.
2. Familiarization of sensor network protocols such as network based and cluster-based protocols.
3. Analysis of issues pertaining to connectivity, coverage and security in a WSN.

Course Outcomes:

Upon completion of this course, students will be able to:

1. Recall the Network Architecture, hardware details, programming tools, Protocols and Special feature of WSN.
2. Demonstrate hardware and Programming Tools for Performance comparison of wireless sensor networks simulation and experimental platforms
3. Analyze Sensor Network Protocols and Security Challenges, Sensor deployment mechanisms.
4. Identify open issues for future research, and enabling technologies in wireless sensor network
5. Design wireless sensor network system for different applications under consideration.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	3	1	3	3	1
CO2	2	1	3	3	1
CO3	3	2	1	3	2
CO4	3	3	2	3	1
CO5	2	2	3	3	3

UNIT-I:

Introduction and overview of sensor network architecture and its applications, SensorNetwork comparison with Ad-Hoc Networks, Sensor node architecture with hardware and software details. Data dissemination and processing; differences compared with other database management systems, data storage; query processing.

UNIT-II:

Hardware: Examples like mica2, mica-Z, telos-B, cricket, Imote2, t-mote, Bt-node, and SunSPOT, Software (Operating Systems): tinyOS, MANTIS, Contiki, and Ret-OS.

UNIT-III:

Programming tools: C, net-C. Performance comparison of wireless sensor networkssimulation and experimental platforms like open source (NS-2) and commercial.

UNIT-IV:

Overview of sensor network protocols (details of at least 2 important protocol per layer):Physical, MAC and routing/ Network layer protocols, node discovery protocols, multi-hop and cluster-based protocols, Fundamentals of 802.15.4, Bluetooth, BLE (Bluetooth low energy), UWB.

UNIT-V:

Specialized features: Energy preservation and efficiency; security challenges; fault tolerance, Issues related to Localization, connectivity and topology, Sensor deployment mechanisms; coverage issues; sensor Web; sensor Grid, Open issues for future research, and Enabling technologies in wireless sensor network.

Text Books:

1. F. Zhao and L. Guibas, “Wireless Sensor Networks: An Information Processing Approach”, Morgan Kaufmann, 1st Indian reprint, 2013.
2. H. Karl and A. Willig, “Protocols and Architectures for Wireless Sensor Networks”, John Wiley & Sons, India, 2012.

Suggested Reading:

1. C. S. Raghavendra, K. M. Sivalingam, and T. Znati, Editors, “Wireless Sensor Networks”, Springer Verlag, 1st Indian reprint, 2010.
2. YingshuLi, MyT. Thai, Weili Wu, “Wireless sensor Network and Applications”, Springer series on signals and communication technology, 2008.

20ME C103

RESEARCH METHODOLOGY AND IPR

(Mandatory Course)

Instruction	2L Hours per week
Duration of SEE	2 Hours
SEE	50 Marks
CIE	25 Marks
Credits	2

Course Objectives:

This course aims to:

1. Motivate to choose research as career
2. Formulate the research problem, prepare the research design
3. Identify various sources for literature review and data collection report writing
4. Equip with good methods to analyze the collected data
5. Know about IPR copyrights

Course Outcomes:

Upon completion of this course, students will be able to:

1. Define research problem, review and asses the quality of literature from various sources
2. Improve the style and format of writing a report for technical paper/ Journal report, understand and develop various research designs
3. Collect the data by various methods: observation, interview, questionnaires
4. Analyze problem by statistical techniques: ANOVA, F-test, Chi-square
5. Understand apply for patent and copyrights

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	3	2	1	2	2
CO2	3	3	3	2	2
CO3	3	2	2	1	2
CO4	3	1	2	2	3
CO5	3	3	3	3	3

UNIT-I

Research Methodology: Research Methodology: Objectives and Motivation of Research, Types of Research, research approaches, Significance of Research, Research Methods verses Methodology, Research Process, Criteria of Good Research, Problems Encountered by Researchers in India, Benefits to the society in general. Defining the Research Problem: Selection of Research Problem, Necessity of Defining the Problem.

UNIT-II

Literature Survey Report Writing: Literature Survey: Importance and purpose of Literature Survey, Sources of Information, Assessment of Quality of Journals and Articles, Information through Internet. Report writing: Meaning of interpretation, layout of research report, Types of reports, Mechanics of writing a report. Research Proposal Preparation: Writing a Research Proposal and Research Report, Writing Research Grant Proposal

UNIT-III

Research Design: Research Design: Meaning of Research Design, Need of Research Design, Feature of a Good Design, Important Concepts Related to Research Design, Different Research Designs, Basic Principles of Experimental Design, Developing a Research Plan, Steps in sample design, types of sample designs.

UNIT-IV

Data Collection and Analysis: Data Collection: Methods of data collection, importance of Parametric, non-parametric test, testing of variance of two normal population, use of Chi-square, ANOVA, Ftest, z-test

UNIT-V

Patents and Copyright: Patent: Macro economic impact of the patent system, Patent document, How to protect your inventions. Granting of patent, Rights of a patent, how extensive is patent protection. Copyright: What is copyright. What is covered by copyright? How long does copyright last? Why protect copyright? Related Rights: what are related rights? Enforcement of Intellectual Property Rights: Infringement of intellectual property rights, Case studies of patents and IP Protection

Text Books:

1. C.R Kothari, “Research Methodology, Methods & Technique”; New Age International Publishers, 2004
2. R. Ganesan, “Research Methodology for Engineers”, MJP Publishers, 2011
3. Y.P. Agarwal, “Statistical Methods: Concepts, Application and Computation”, Sterling Publs., Pvt., Ltd., New Delhi, 2004

Suggested Reading:

1. AjitParulekar and Sarita D’ Souza, “Indian Patents Law – Legal & Business Implications”; Macmillan India ltd, 2006
2. B. L.Wadehra; “Law Relating to Patents, Trade Marks, Copyright, Designs & Geographical Indications”; Universal law Publishing Pvt. Ltd., India 2000.
3. P. Narayanan; “Law of Copyright and Industrial Designs”; Eastern law House, Delhi 2010.

20CE A101

DISASTER MANAGEMENT

(Audit Course)

Instruction	2L Hours per week
Duration of SEE	2 Hours
SEE	50 Marks
CIE	--
Credits	Non-Credit

Course Objectives:

This course aims to:

1. Equip the students with the basic knowledge of hazards, disasters, risks and vulnerabilities including natural, climatic and human induced factors and associated impacts
2. Impart knowledge in students about the nature, causes, consequences and mitigation measures of the various natural disasters
3. Enable the students to understand risks, vulnerabilities and human errors associated with human induced disasters
4. Enable the students to understand and assimilate the impacts of any disaster on the affected area depending on its position/ location, environmental conditions, demographic, etc.
5. Equip the students with the knowledge of the chronological phases ina disaster management cycle and to create awareness about the disaster management framework and legislations in the context of national and global conventions

Course Outcomes:

Upon completion of this course, students will be able to:

1. Ability to analyze and critically examine existing programs in disaster management regarding vulnerability, risk and capacity at different levels
2. Ability to understand and choose the appropriate activities and tools and set up priorities to build a coherent and adapted disaster management plan
3. Ability to understand various mechanisms and consequences of human induced disasters for the participatory role of engineers in disaster management
4. Understand the impact on various elements affected by the disaster and to suggest and apply appropriate measures for the same
5. Develop an awareness of the chronological phases of disaster preparedness, response and relief operations for formulating effective disaster management plans and ability to understand various participatory approaches/strategies and their application in disaster management

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	2	3	2	1	1
CO2	3	3	2	2	2
CO3	2	3	3	2	2
CO4	3	3	2	3	3
CO5	3	2	2	3	3

UNIT-I

Introduction: Basic definitions- Hazard, Disaster, Vulnerability, Risk, Resilience, Mitigation, Management; classification of types of disaster- Natural and man- made; International Decade for natural disaster reduction (IDNDR); International strategy for disaster reduction (ISDR), National disaster management authority (NDMA).

UNIT-II

Natural Disasters: Hydro meteorological disasters: Causes, Early warning systems- monitoring and management, structural and non-structural measures for floods, drought and Tropical cyclones; Geographical based disasters: Tsunami generation, causes, zoning, Early warning systems- monitoring and management, structural and non-structural mitigation measures for earthquakes, tsunami, landslides, avalanches and forest fires. Case studies related to various hydro meteorological and geographical based disasters.

UNIT-III

Human Induced Hazards: Chemical disaster- Causes, impacts and mitigation measures for chemical accidents, Risks and control measures in a chemical industry, chemical disaster management; Case studies related to various chemical industrial hazards eg: Bhopal gas tragedy; Management of chemical terrorism disasters and biological disasters; Radiological Emergencies and case studies; Case studies related to major power break downs, fire accidents, traffic accidents, oil spills and stampedes, disasters due to double cellar construction in multi- storied buildings.

UNIT-IV

Disaster Impacts: Disaster impacts- environmental, physical, social, ecological, economical, political, etc.; health, psycho-social issues; demographic aspects- gender, age, special needs; hazard locations; global and national disaster trends; climate change and urban disasters.

UNIT-V

Concept of Disaster Management: Disaster management cycle – its phases; prevention, mitigation, preparedness, relief and recovery; risk analysis, vulnerability and capacity assessment; Post-disaster environmental response- water, sanitation, food safety, waste management, disease control; Roles and responsibilities of government, community, local institutions, NGOs and otherstakeholders; Policies and legislation for disaster risk reduction, DRR Programs in India and the activities of National Disaster Management Authority.

Text Books:

1. Pradeep Sahni," Disaster Risk Reduction in South Asia", Prentice Hall, 2003.
2. B. K. Singh," Handbook of Disaster Management: techniques & Guidelines", Rajat Publication, 2008.

Suggested Reading:

1. Ministry of Home Affairs". Government of India, "National disaster management plan, Part I and II",
2. K. K. Ghosh," Disaster Management", APH Publishing Corporation, 2006.
3. http://www.indiaenvironmentportal.org.in/files/file disaster_management_india1.pdf
4. http://www.ndmindia.nic.in/ (National Disaster management in India, Ministry of Home Affairs)
5. Hazards, Disasters and your community: A booklet for students and the community, Ministry of home affairs.

20EG A101

ENGLISH FOR RESEARCH PAPER WRITING

(Audit Course)

Instruction	2L Hours per week
Duration of SEE	2 Hours
SEE	50 Marks
CIE	--
Credits	Non-Credit

Course Objectives:

This course aims to:

1. To the various purposes of Research Papers and help them infer the benefits and limitations of research.
2. To developing the content, formulating a structure and illustrating the format of writing a research paper.
3. In differentiating between qualitative and quantitative research types.
4. To constructing paragraphs and developing thesis statement.
5. To producing original research papers while avoiding plagiarism.

Course Outcomes:

Upon completion of this course, students will be able to:

1. Illustrate the nuances of research paper writing and draw conclusions about the benefits and limitations of research.
2. Classify different types of research papers and organize the format and citation of sources.
3. Review the literature and categorize between different types of research.
4. Draft paragraphs and write thesis statement in a scientific manner.
5. Develop an original research paper while acquiring the knowledge of how and where to publish their papers.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	2	2	2	1	2
CO2	3	3	1	1	1
CO3	3	3	2	1	1
CO4	3	3	1	1	1
CO5	3	3	2	1	1

UNIT-I

Academic Writing

Meaning & Definition of a research paper– Purpose of a research paper – Scope – Benefits – Limitations – outcomes.

UNIT-II

Research Paper Format

Title – Abstract – Introduction – Discussion – Findings – Conclusion – Style of Indentation – Font size/Font types – Indexing – Citation of sources.

UNIT-III

Research Methodology

Methods (Qualitative – Quantitative) Review of Literature. Criticizing, Paraphrasing & Plagiarism.

UNIT-IV

Process of Writing a Research Paper

Choosing a topic - Thesis Statement – Outline – Organizing notes - Language of Research – Word order, Paragraphs – Writing first draft–Revising/Editing - The final draft and proof reading. IEEE Style.

UNIT-V

Research Paper Publication

Reputed Journals – National/International – ISSN No, No. of volumes, Scopus Index/UGC Journals – Free publications - Paid Journal publications – /Advantages/Benefits

Text Book:

1. C. R Kothari, Gaurav, Garg, Research Methodology Methods and Techniques, New Age International Publishers. 4th Edition.

Suggested Reading:

1. Day R, "How to Write and Publish a Scientific Paper", Cambridge University Press, 2006.
2. MLA "Hand book for writers of Research Papers", East West Press Pvt. Ltd, New Delhi, 7th Edition.
3. Lipson, Charles (2011), Cite Right: A Quick Guide to Citation Styles; MLA, APA, Chicago, The Sciences, Professions, and more (2nd Edition). Chicago [u.a] : Univ of Chicago Press.

Online Resources:

1. NPTEL: https://onlinecourses.nptel.ac.in/noc18_mg13/preview
2. NPTEL: https://nptel.ac.in/courses/121/106/121106007/
3. https://www.classcentral.com/course/swayam-introduction-to-research-5221

20EGA102

INDIAN CONSTITUTION AND FUNDAMENTAL RIGHTS

(Audit Course)

Instruction	2L Hours per week
Duration of SEE	2 Hours
SEE	50 Marks
CIE	--
Credits	Non-Credit

Course Objectives:

This course aims to:

1. The history of Indian Constitution and its role in the Indian democracy.
2. Address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
3. Have knowledge of the various Organs of Governance and Local Administration.

Course Outcomes:

Upon completion of this course, students will be able to:

1. Understand the making of the Indian Constitution and its features.
2. Understand the Rights of equality, the Right of freedom and the Right to constitutional remedies.
3. Have an insight into various Organs of Governance - composition and functions.
4. Understand powers and functions of Municipalities, Panchayats and Co-operative Societies.
5. Understand Electoral Process, special provisions.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	2	-	-	-	2
CO2	2	-	-	-	2
CO3	2	-	-	1	2
CO4	2	-	-	1	2
CO5	2	-	-	1	2

UNIT-I

History of Making of the Indian Constitutions: History, Drafting Committee (Composition &Working). Philosophy of the Indian Constitution: Preamble, Salient Features.

UNIT-II

Contours of Constitutional Rights and Duties: Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

UNIT-III

Organs of Governance: Parliament: Composition, Qualifications, Powers and Functions

Union executives: President, Governor, Council of Ministers, Judiciary, appointment and transfer of judges, qualifications, powers and functions

UNIT-IV

Local Administration: District's Administration head: Role and importance. Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Panchayati Raj: Introduction, PRIZilla Panchayat, Elected Officials and their roles, CEO Zilla Panchayat: positions and role. Block level: Organizational Hierarchy (Different departments) Village level: role of elected and appointed officials. Importance of grass root democracy.

UNIT-V

Election Commission: Election Commission: Role and functioning, Chief Election Commissioner and Election Commissioners, State Election Commission: Role and functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.

Text Books:

1. The Constitution of India, 2050 (Bare Act), GovernmentPublication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar, Framing of Indian Constitution, 1st Edition,2015.
3. M. P. Jain, Indian Constitution Law, 7th Edition., Lexis Nexis,2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis,2015.

Online Resources:

1. http://www.nptel.ac.in/courses/103106084/Script.pdf

20IT A101

PEDAGOGY STUDIES

(Audit Course)

Instruction	2L Hours per week
Duration of SEE	2 Hours
SEE	50 Marks
CIE	--
Credits	Non-Credit

Course Objectives:

This course aims to:

1. Present the basic concepts of design and policies of pedagogy studies.
2. Provide understanding of the abilities and dispositions with regard to teaching techniques, curriculum design and assessment practices.
3. Familiarize various theories of learning and their connection to teaching practice.
4. Create awareness about the practices followed by DFID, other agencies and other researchers.
5. Provide understanding of critical evidence gaps that guides the professional development.

Course Outcomes:

Upon completing this course, students will be able to:

1. Illustrate the pedagogical practices followed by teachers in developing countries both in formal and informal classrooms.
2. Examine the effectiveness of pedagogical practices.
3. Understand the concept, characteristics and types of educational research and perspectives of research.
4. Describe the role of classroom practices, curriculum and barriers to learning.
5. Understand Research gaps and learn the future directions.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	1	1	1	2	2
CO2	1	1	1	2	2
CO3	2	2	2	2	2
CO4	1	1	1	2	2
CO5	2	2	2	2	2

UNIT-I

Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology - Theories of learning, Curriculum, Teacher education - Conceptual framework, Research questions - Overview of methodology and Searching.

UNIT-II

Thematic Overview: Pedagogical practices followed by teachers in formal and informal classrooms in developing countries - Curriculum, Teacher education.

UNIT-III

Evidence on the Effectiveness of Pedagogical Practices: Methodology for the in-depth stage: quality assessment of included studies - How can teacher education (curriculum and Practicum) and the school curriculum and guidance material best support effective pedagogy? - Theory of change - Strength and nature of the body of evidence for effective pedagogical practices - Pedagogic theory and pedagogical approaches - Teachers' attitudes and beliefs and pedagogic strategies.

UNIT-IV

Professional Development: alignment with classroom practices and follow up support - Support from the head teacher and the community – Curriculum and assessment - Barriers to learning: Limited resources and large class sizes.

UNIT-V

Research Gaps and Future Directions: Research design – Contexts – Pedagogy - Teacher education - Curriculum and assessment – Dissemination and research impact.

Text Books:

1. Ackers J, Hardman F, "Classroom Interaction in Kenyan Primary Schools, Compare", 31 (2): 245 – 261, 2001.
2. Agarwal M, "Curricular Reform in Schools: The importance of evaluation", Journal of Curriculum Studies, 36 (3): 361 – 379, 2004.

Suggested Reading:

1. Akyeampong K, "Teacher Training in Ghana – does it count? Multisite teacher education research project (MUSTER)", Country Report 1. London: DFID, 2003.
2. Akyeampong K, Lussier K, Pryor J, Westbrook J, "Improving teaching and learning of Basic Maths and Reading in Africa: Does teacher Preparation count? International Journal Educational Development, 33 (3): 272- 282, 2013.
3. Alexander R J, "Culture and Pedagogy: International Comparisons in Primary Education", Oxford and Boston: Blackwell, 2001.
4. Chavan M, "Read India: A mass scale, rapid, 'learning to read' campaign", 2003.

Web Resources:

1. https://onlinecourses.nptel.ac.in/noc17_ge03/preview
2. www.pratham.org/images/resources%20working%20paper%202.pdf.

20EG A104

PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTMENT SKILLS

(Audit Course)

Instruction	2 LHours per week
Duration of SEE	2 Hours
SEE	50 Marks
CIE	--
Credits	Non-Credit

Course Objectives:

This course aims to:

1. Learn to achieve the highest goal happily.
2. Become a person with stable mind, pleasing personality and determination.
3. Awaken wisdom among themselves.

Course Outcomes:

Upon completing this course, students will be able to:

1. Develop their personality and achieve their highest goal of life.
2. Lead the nation and mankind to peace and prosperity.
3. To practice emotional self-regulation.
4. Develop a positive approach to work and duties.
5. Develop a versatile personality.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	2	1	-	-	2
CO2	2	1	-	-	2
CO3	2	1	-	-	2
CO4	2	1	-	-	2
CO5	2	1	-	-	2

UNIT-I

Neetisatakam – Holistic Development of Personality - Verses 20, 20, 21, 22 (Wisdom) - Verses 29, 31, 32 (Pride and Heroism) - Verses 26,28,63,65 (Virtue)

UNIT-II

Neetisatakam – Holistic Development of Personality (cont'd) - Verses 52, 53, 59 (dont's) - Verses 71,73,75 & 78 (do's) - Approach to day to day works and duties.

UNIT-III

Introduction to Bhagavad Geetha for Personality Development - Shrimad Bhagawad Geeta: Chapter 2 – Verses 41, 47, 48 - Chapter 3 – Verses 13,21,27,35-Chapter6–Verses5,13,17,23,35-Chapter18–Verses45, 46, 48Chapter – 6: Verses 5, 13, 17, 23, 35; Chapter – 18: Verses 45, 46, 48

UNIT-IV

Statements of Basic Knowledge - Shrimad Bhagawad Geeta: Chapter 2- Verses 56, 62,68 - Chapter 12 – Verses 13, 14, 15, 16, 17, 18 - Personality of Role model from Shrimad Bhagawat Geeta.

UNIT-V

Role of Bhagavad Geeta in the Present Scenario - Chapter 2 – Verses 17 - Chapter 3 – Verses 36, 37, 42 - Chapter 4 – Verses 18, 38, 39 - Chapter 18 – Verses37, 38, 63.

Text Books:

1. "Srimad Bhagavad Gita" by Swami SwarupanandaAdvaita Ashram (Publication Department), Kolkata
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi

Suggested Reading:

1. NTPEL: http://nptel.ac.in/downloads/109104115/

20EE A101

SANSKRIT FOR TECHNICAL KNOWLEDGE

(Audit Course)

Instruction	2 L Hours per week
Duration of SEE	2 Hours
SEE	50 Marks
CIE	--
Credits	Non-Credit

Course Objectives:

This course aims to:

1. Get a working knowledge in illustrious Sanskrit, the scientific language in the world
2. Make the novice Learn the Sanskrit to develop the logic in mathematics, science & other subjects
3. Explore the huge knowledge from ancient Indian literature

Course Outcomes:

Upon completing this course, students will be able to:

1. Develop passion towards Sanskrit language
2. Decipher the latent engineering principles from Sanskrit literature
3. Correlates the technological concepts with the ancient Sanskrit history.
4. Develop knowledge for the technological progress
5. Explore the avenue for research in engineering with aid of Sanskrit.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	1	1	1	1	1
CO2	2	1	1	1	1
CO3	2	1	1	1	1
CO4	2	1	1	1	1
CO5	1	1	1	1	1

UNIT-I

Introduction to Sanskrit Language: Sanskrit Alphabets-vowels-consonants- significance of Amarakosa-parts of speech-Morphology-creation of new words- significance of synonyms-sandhi-samasa-sutras-active and passive voice-Past/ Present/Future Tense-syntax-Simple Sentences (elementary treatment only)

UNIT-II

Role of Sanskrit in Basic Sciences: Brahmagupthas lemmas (second degree indeterminate equations), sum of squares of n-terms of AP- sulba_sutram or baudhayana theorem (origination of pythogorous theorem)-value of pie- Madhava's sine and cosine theory (origination of Taylor's series). The measurement system-time-mass-length-temp, Matter elasticity-optics-speed of light (origination of michealson and morley theory).

UNIT-III

Role of Sanskrit in Engineering-I (Civil, Mechanical, Electrical and Electronics Engineering): Building construction-soil testing-mortar-town planning-Machine definition-crucible-furnace-air blower-Generation of electricity in a cell- magnetism-Solar system-Sun: The source of energy, the earth-Pingala chandasutram (origination of digital logic system)

UNIT-IV

Role of Sanskrit in Engineering-II (Computer Science Engineering & Information Technology): Computer languages and the Sanskrit languages- computer command words and the vedic command words-analogy of pramana in memamsa with operators in computer language-sanskrit analogy of physical sequence and logical sequence, programming.

UNIT-V

Role of Sanskrit in Engineering-III (Bio-technology and Chemical Engineering): Classification of plants-plants, the living-plants have senses-classification of living creatures Chemical laboratory location and layout-equipment-distillation vessel- kosthiyanthram

Text Books:

1. M Krishnamachariar, History of Classical Sanskrit Literature, TTD Press, 2037.
2. M.R. Kale, A Higher Sanskrit Grammar: For the Use of School and College Students, Motilal Banarsidass Publishers, ISBN-13: 978- 8120801783, 2015
3. Kapil Kapoor, Language, Linguistics and Literature: The Indian Perspective, ISBN-10: 8171880649, 2094.
4. Pride of India, Samskrita Bharati Publisher, ISBN: 81-87276-27-4, 2007
5. Shri RamaVerma, Vedas the source of ultimate science, Nag publishers, ISBN:81-6081-618-1, 2005

20EG A103

STRESS MANAGEMENT BY YOGA

(Audit Course)

Instruction	2 L Hours per Week
Duration of SEE	2 Hours
SEE	50 Marks
CIE	--
Credits	Non-Credit

Course Objectives:

This course aims to:

1. Creating awareness about different types of stress and the role of yoga in the management of stress.
2. Promotion of positive health and overall wellbeing (Physical, mental, emotional, social and spiritual).
3. Prevention of stress related health problems by yoga practice.

Course Outcomes:

Upon completing this course, students will be able to:

1. Understand yoga and its benefits.
2. Enhance Physical strength and flexibility.
3. Learn to relax and focus.
4. Relieve physical and mental tension through asanas
5. Improve work performance and efficiency.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	2	1	-	-	1
CO2	2	1	-	-	1
CO3	2	1	-	-	1
CO4	2	1	-	-	1
CO5	2	1	-	-	1

UNIT-I

Meaning and Definition of Yoga - Historical perspective of Yoga - Principles of Astanga Yoga by Patanjali.

UNIT–II

Meaning and Definition of Stress - Types of stress - Eustress and Distress. Anticipatory Anxiety and Intense Anxiety and depression. Meaning of Management- Stress Management.

UNIT-III

Concept of Stress According to Yoga - Stress assessment methods - Role of Asana, Pranayama and Meditation in the management of stress.

UNIT-IV

Asanas- (5 Asanas in each posture) - Warm up - Standing Asanas - Sitting Asanas - Prone Asanas - Supine asanas - Surya Namaskar

UNIT-V

Pranayama- Anulom and Vilom Pranayama - Nadishudhi Pranayama - Kapalabhati Pranayama - Bhramari Pranayama - Nadanusandhana Pranayama. Meditation Techniques: Om Meditation - Cyclic meditation: Instant Relaxation technique (QRT), Quick Relaxation Technique (QRT), Deep Relaxation Technique (DRT)

Text Books:

1. "Yogic Asanas for Group Training - Part-I": Janardhan Swami Yogabhyasi Mandal, Nagpur.
2. "Rajayoga or Conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication
   Department), Kolkata.
3. Nagendra H.R and Nagaratna R, "Yoga Perspective in Stress Management", Bangalore, Swami Vivekananda Yoga Prakashan

Suggested Reading:

1. https://onlinecourses.nptel.ac.in/noc16_ge04/preview
2. https://freevideolectures.com/course/3539/indian-philosophy/11

20EC A101

VALUE EDUCATION

(Audit Course)

Instruction	2 L Hours per Week
Duration of SEE	2 Hours
SEE	50 Marks
CIE	--
Credits	Non-Credit

Course Objectives:

This course aims to

1. Understand the need and importance of Values for self-development and for National development.
2. Imbibe good human values and Morals
3. Cultivate individual and National character.

Course outcomes:

After completion of the Course, Students will be able to

1. Summarize classification of values and values for self-development.
2. Identify the importance of values in personal and professional life.
3. Apply the importance of social values for better career and relationships.
4. Compile the values from holy books for personal and social responsibility.
5. Discuss concept of soul and reincarnation, values Dharma, Karma and Guna.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	2	2	2	2	3
CO2	2	2	2	2	3
CO3	2	2	2	2	3
CO4	2	2	2	2	3
CO5	2	2	2	2	3

UNIT-I

Human Values, Ethics and Morals: Concept of Values, Indian concept of humanism, human values; Values for self-development, Social values, individual attitudes; Work ethics, moral and non- moral behavior, standards and principles based on religion, culture and tradition.

UNIT-II

Value Cultivation, and Self-Management: Need and Importance of cultivation of values such as Sense-of Duty, Devotion to work, Self-reliance, Confidence, Concentration, Integrity & discipline, and Truthfulness.

UNIT-III

Spiritual Outlook and Social Values: Personality and Behavior, Scientific attitude and Spiritual (soul) outlook; Cultivation of Social Values Such as Positive Thinking, Punctuality, Love & Kindness, avoiding

fault finding in others, Reduction of anger, forgiveness, Dignity of labor, True friendship, Universal brotherhood and religious tolerance.

UNIT-IV

Values in Holy Books: Self-management and Good health; **and internal & external Cleanliness,** Holy books versus Blind faith, Character and Competence, Equality, Nonviolence, Humility, Role of Women.

UNIT-V

Dharma, Karma and Guna: Concept of soul; Science of Reincarnation, Character and Conduct, Concept of Dharma; Cause and Effect based Karma Theory; The qualities of Devine and Devilish; Satwic, Rajasic and Tamasic gunas.

Text Books:

1. Chakroborty, S.K. “Values & Ethics for organizations Theory and practice”, Oxford University Press, New Delhi, 2098.
2. Jaya DayalGoyandaka, “Srimad Bhagavad Gita”, withSanskrit Text, Word meaning and Prose meaning, Gita Press, Gorakhpur, 2017.

20CS O101

BUSINESS ANALYTICS

(Open Elective)

Instruction	3 L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Course Objectives:

This course aims to:

1. Understanding the basic concepts of business analytics and applications
2. Study various business analytics methods including predictive, prescriptive and prescriptive analytics
3. Prepare the students to model business data using various data mining, decision making methods

Course Outcomes:

Upon completing this course, students will be able to:

1. Identify and describe complex business problems in terms of analytical models.
2. Apply appropriate analytical methods to find solutions to business problems that achieve stated objectives.
3. Interpret various metrics, measures used in business analytics
4. Illustrate various descriptive, predictive and prescriptive methods and techniques
5. Model the business data using various business analytical methods and techniques

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	3	2	2	1	1
CO2	3	3	2	-	3
CO3	3	3	3	-	-
CO4	3	3	3	-	-
CO5	3	3	3	-	-

UNIT-I

Introduction to Business Analytics: Introduction to Business Analytics, need and science of data driven (DD) decision making, Descriptive, predictive, prescriptive analytics and techniques, Big data analytics, Web and Social media analytics, Machine Learning algorithms, framework for decision making, challenges in DD decision making and future.

UNIT-II

Descriptive Analytics: Introduction, data types and scales, types of measurement scales, population and samples, measures of central tendency, percentile, decile and quadrille, measures of variation, measures of shape-skewness, data visualization.

UNIT-III

Forecasting Techniques: Introduction, time-series data and components, forecasting accuracy, moving average method, single exponential smoothing, Holt's method, Holt-Winter model, Croston's forecasting method, regression model for forecasting, Auto regression models, auto-regressive moving process, ARIMA, Theil's coefficient

UNIT-IV

Decision Trees: CHAID, Classification and Regression tree, splitting criteria, Ensemble and method and random forest. Clustering: Distance and similarity measures used in clustering, Clustering algorithms, K-Means and Hierarchical algorithms, Prescriptive Analytics- Linear Programming (LP) and LP model building,

UNIT-V

Six Sigma: Introduction, introduction, origin, 3-Sigma Vs Six-Sigma process, cost of poor quality, sigma score, industry applications, six sigma measures, DPMO, yield, sigma score, DMAIC methodology, Six Sigma toolbox

Text Books:

1. U Dinesh Kumar, "Data Analytics", Wiley Publications, 1st Edition, 2017
2. Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, "Business analytics Principles, Concepts, and Applications with SAS", Associate Publishers, 2015.

Suggested Reading:

1. S. Christian Albright, Wayne L. Winston, "Business Analytics - Data Analysis and Decision Making", 5thEdition, Cengage, 2015.

Web Resources:

1. https://onlinecourses.nptel.ac.in/noc18-mg11/preview
2. https://nptel.ac.in/courses/110105089/

20MEO103

COMPOSITE MATERIALS

(Open Elective)

Instruction	3L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Course Objectives:

This course aims to:

1. Composite materials and their constituents.
2. Classification of the reinforcements and evaluate the behavior of composites.
3. Fabrication methods of metal matrix composites.
4. Manufacturing of Polymer matrix composites.
5. Failure mechanisms in composite materials.

Course Outcomes:

Upon completing this course, students will be able to:

1. Classify and characterize the composite materials.
2. Describe types of reinforcements and their properties.
3. Understand different fabrication methods of metal matrix composites.
4. Understand different fabrication methods of polymer matrix composites.
5. Decide the failure of composite materials.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	3	1	3	1	1
CO2	3	1	3	1	1
CO3	3	2	3	1	1
CO4	3	2	3	1	1
CO5	3	1	3	1	1

UNIT–I

Introduction: Definition, classification and characteristics of composite materials, advantages and application of composites, functional requirements of reinforcement and matrix, effect of reinforcement (size, shape, distribution, volume fraction) on over all composite performance.

UNIT–II

Reinforcements: Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, kevlar fibers and boron fibers, properties and applications of whiskers, particle reinforcements, mechanical behavior of composites, rule of mixtures, inverse rule of mixtures, isostrain and isostress conditions.

UNIT–III

Manufacturing of metal matrix composites: Casting, solid state diffusion technique, cladding, hot isostatic pressing, properties and applications.

Manufacturing of ceramic matrix composites: liquid metal infiltration, liquid phase sintering.

Manufacturing of carbon–carbon composites: knitting, braiding, weaving, properties and applications.

UNIT-IV

Manufacturing of Polymer Matrix Composites: Preparation of moulding compounds and prepregs, hand layup method, autoclave method, filament winding method, compression moulding, reaction injection moulding, properties and applications.

UNIT-V

Strength: Lamina failure criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure, laminate first play failure, insight strength.

Text Books:

1. Deborah D.L. Chung "Composite materials: Science and applications", Springer 2/e, 2010.
2. WD Callister, Jr., adapted by R. Balasubramaniam, "Materials science and engineering, an introduction"., John Wiley & sons, NY, Indian edition, 2/e, 2007.
3. R.M. Jones, "Mechanics of composite materials", 2/e, Mc Graw Hill co., 2098.

Suggested Reading:

1. K.K.Chawla, 4/e "Composite materials", Springer Book Archives, 2020.
2. Daniel Gay, Suong V. Hoa, and Stephen W. Tsai, "Composite materials design and applications", CRC press, 2015.

20CEO101

COST MANAGEMENT OF ENGINEERING PROJECTS

(Open Elective)

Instruction	3 L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Course Objectives:

This course aims to:

1. Enable the students to understand the concepts of Project management.
2. Provide knowledge on concepts of Project Planning and scheduling.
3. Create an awareness on Project Monitoring and Cost Analysis
4. Provide adequate knowledge to the students on Recourse Management Costing-Variance Analysis
5. Train the students with the concepts of Budgetary Control for cost management and to provide basic platform on Quantitative techniques for cost management.

Course Outcomes:

Upon completing this course, students will be able to:

1. Acquire in-depth knowledge about the concepts of project management and understand the principles of project management.
2. Determine the critical path of a typical project using CPM and PERT techniques.
3. Prepare a work break down plan and perform linear scheduling using various methods.
4. Solve problems of resource scheduling and levelling using network diagrams.
5. Learn the concepts of budgetary control and apply quantitative techniques for optimizing project cost.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	1	2	1	2	1
CO2	1	2	1	1	1
CO3	3	2	2	1	1
CO4	3	2	2	1	1
CO5	1	1	1	1	1

UNIT-I

Project Management: Introduction to project managements, stakeholders, roles, responsibilities and functional relationships. Principles of project management, objectives and project management system. Project team, organization, roles, and responsibilities. Concepts of project planning, monitoring, staffing, scheduling and controlling.

UNIT-II

Project Planning and Scheduling: Introduction for project planning, defining activities and their interdependency, time and resource estimation. Work break down structure. Linear scheduling methods-

bar charts, Line of Balance (LOB), their limitations. Principles, definitions of network-based scheduling methods: CPM, PERT. Network representation, network analysis-forward and backward passes.

UNIT-III

Project Monitoring and Cost Analysis: Introduction-Cost concepts in decision- making; Relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision-Making, Time cost tradeoff- Crashing project schedules, its impact on time on time, cost. Project direct and indirect costs.

UNIT-IV

Resources Management and Costing-Variance Analysis: Planning, Enterprise Resource Planning, Resource scheduling and levelling. Total Quality Management and Theory of constraints. Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis Standard Costing and Variance Analysis. Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector. Just-in-time approach, Material Requirement

UNIT-V

Budgetary Control: Flexible Budgets; Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing. Quantitative Techniques for Cost Management: Linear Programming, PERT/ CPM, Transportation Assignment problems, Simulation, Learning Curve Theory.

Text Books:

1. Charles T Horngren “Cost Accounting A Managerial Emphasis”, Pearson Education; 14th edition 2012,
2. Charles T. Horngren and George Foster, “Advanced Management Accounting” Prentice-Hall; 6th Revised edition, 2087
3. Robert S Kaplan Anthony A. Atkinson, “Management & Cost Accounting” , Pearson; 2nd edition, 2096
4. K. K Chitkara, “Construction Project Management: Planning, scheduling and controlling”, Tata McGraw-Hill Education. 2004.
5. Kumar Neeraj Jha “Construction Project Management Theory and Practice”, Pearson Education India; 2nd edition, 2015.

20ME O101

INDUSTRIAL SAFETY

(Open Elective)

Instruction	3L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Course Objectives:

This course aims to:

1. Causes for industrial accidents and preventive steps to be taken.
2. Fundamental concepts of maintenance engineering.
3. About wear and corrosion along with preventive steps to be taken.
4. The basic concepts and importance of fault tracing.
5. The steps involved in carrying out periodic and preventive maintenance of various equipments used in industry.

Course Outcomes:

Upon completion of this course, students will be able to:

1. Identify the causes for industrial accidents and suggest preventive measures for safety.
2. Understand the basic need and requirements of different maintenance procedures.
3. Apply different techniques to reduce and prevent wear and corrosion in industry.
4. Analyze different types of faults present in various equipments like machine tools, IC engines, boilers etc.
5. Formulate a plan for periodic and preventive maintenance techniques as required for industrial equipments like motors, pumps and air compressors.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	3	3	3	3	2
CO2	3	3	3	2	2
CO3	3	1	3	2	1
CO4	3	1	3	2	1
CO5	3	2	3	3	3

UNIT – I

Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 2048 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, safety color codes, fire prevention and firefighting, equipment and methods.

Workplace safety standards during pandemic: workplace safety requirements mandating appropriate personal protective equipment, sanitation, social distancing, infectious disease preparedness and response plans, record keeping, training, and hazard communications in workplaces safety.

UNIT – II

Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, primary and secondary functions and responsibility of maintenance
department, types of maintenance, types and applications of tools used for maintenance, maintenance cost & its relation with replacement economy, service life of equipment.

UNIT – III

Wear: Types, causes, effects, wear reduction methods.

Lubrication: Types and applications, lubrication methods, general sketch, working and applications of screw down grease cup, pressure grease gun, splash lubrication, gravity lubrication, wick feed lubrication, side feed lubrication, ring lubrication.

Corrosion and prevention: Definition of corrosion, principle and factors affecting the corrosion, types of corrosion, corrosion prevention methods.

UNIT–IV

Fault tracing: Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment's like, any one machine tool, pump, air compressor, internal combustion engine, boiler, electrical motors, types of faults in machine tools and their general causes.

UNIT – V

Periodic and Preventive Maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components and electric motors. Periodic and preventive maintenance of machine tools, pumps, air compressors, diesel generator sets.

Text books:

1. H. P. Garg, "Maintenance engineering", S. Chand & co, 2010.
2. Tyler G. Hicks and T. W. Edwards, "Pump application engineering", Mc Graw Hill, 2071.
3. Roger L Brauer, "Safety and health for engineers', Wiley-Interscience& Sons, 2016.

Suggested Readings:

1. Higgins & Morrow, "Maintenance engineering handbook", 3rd edition, Mc Graw Hill, 2077.
2. Winterkorn, Hans, "Foundation engineering handbook", Chapman & Hall, London, 2075.

20ME O102

INTRODUCTION TO OPTIMIZATION TECHNIQUES

(Open Elective)

Instruction	3 L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Course Objectives:

This course aims to:

1. Come to know the formulation of LPP models.
2. Understand the transportation and assignment techniques.
3. Come to know the procedure of project management along with CPM and PERT techniques.
4. Understand the concepts of queuing theory and inventory models.
5. Understand sequencing techniques.

Course Outcomes:

Upon completing this course, students will be able to:

1. Build and Solve the linear programming problems.
2. Solve the given transportation problem.
3. Analyze project management techniques like CPM and PERT to plan and execute projects successfully.
4. Compare various inventory control techniques.
5. Apply sequencing and queuing theory concepts for industry applications.

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	3	1	3	1	2
CO2	3	1	3	1	2
CO3	1	1	3	2	3
CO4	2	1	3	2	2
CO5	2	1	3	3	2

UNIT - I

Operations Research: Definition, scope, Models, Linear programming problems (LPP), Formulation, Graphical Method, and Simplex Method

UNIT - II

Transportation Models: Finding an initial feasible solution - North West Corner Method, Least Cost Method, Vogel's Approximation Method, Finding the optimal solution, Special cases in Transportation problems - Unbalanced Transportation problem, Degeneracy in Transportation, Profit Maximization in Transportation.

UNIT- III

Project Management: Definition, Procedure and Objectives of Project Management, Differences between PERT and CPM, Rules for drawing Network diagram, Scheduling the activities, Fulkerson's rule, Earliest and Latest times, Determination of ES and EF times in forward path, LS & LF times in backward path, Determination of critical path, duration of the project, Free float, Independent float and Total float

UNIT - IV

Queuing Theory and Inventory: Kendols Notation, single server models, Inventory control - deterministic inventory models - Probabilistic inventory control models.

UNIT - V

Sequencing Models: Introduction, Objectives, General assumptions, processing 'n' jobs through two Machines, processing 'n' jobs through three machines.

Text Books:

1. H.A. Taha, "Operations research", 10th edition, Prentice Hall of India, New Delhi, 2017.
2. S. D. Sharma, Himanshu Sharma, "Operations research: Theory, methods and applications", 15th edition, Kedar Nath Ram Nath, 2010
3. Dr. D. S. Hira, Er. Prem Kumar Gupta, "Operations research", S. Chand & company ltd,2014

Suggested Reading:

1. Hillier F.S. and Lieberman G.J., "Introduction to operations research", 7th Edition, TMH, 2009
2. Rao. S. S., "Optimization theory and applications", 2nd edition, Wiley Eastern ltd., 2004.

20EE O101

WASTE TO ENERGY

(Open Elective)

Instruction	3 L Hours per Week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

Course Objectives:

This course aims to:

1. Know the various forms of waste
2. Understand the processes of Biomass Pyrolysis.
3. Learn the technique of Biomass Combustion.

Course Outcomes:

Upon completing this course, students will be able to:

1. Understand the concept of conservation and Identify the devices for conservation
2. Classify the different forms of wastage
3. Explain the process of Gasification, Demonstrate the design and operation of Gasifiers
4. Explain the process of Combustion, Demonstratethe construction and operation of various combustors
5. Describe the process of biomass conversion and to Differentiate biomass, biogas, biochemical and biodiesel plants

CO.NO	PO1	PO2	PO3	PO4	PO5
CO1	1	1	1	1	1
CO2	2	1	1	1	2
CO3	2	1	1	1	2
CO4	1	1	1	1	1
CO5	2	2	1	1	2

UNIT-I

Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors.

UNIT-II

Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

UNIT-III

Biomass Gasification: Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation.

UNIT-IV

Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

UNIT-V

Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy Program in India.

Text Books:

1. Desai, Ashok V, "Non-Conventional Energy", Wiley Eastern Ltd., 2090.
2. Khandelwal, K. C. and Mahdi, S. S, "Biogas Technology - A Practical Hand Book", Vol. I &II, Tata McGraw Hill Publishing Co. Ltd., 2083.

Suggested Reading:

1. Challal, D. S., "Food, Feed and Fuel from Biomass", IBH Publishing Co. Pvt. Ltd., 2091.
2. C. Y. WereKo-Brobby and E. B. Hagan, "Biomass Conversion and Technology", John Wiley & Sons, 2096.